EPFL

Modularity through Memory Virtualization

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School of Computer & Communication Sciences

Objectives

Objectives

- Understand memory virtualization
  - *the coolest form of modularization we have in operating systems*
- Back-of-the-envelope calculations
  - *sanity-check a design before writing any code*

Outline

- Names and Page Tables
  - *PT = directory for mapping memory names (VA) to memory locations (PA)*
  - *Specific example: Intel Skylake microarchitecture*
- Caching
  - *Generalities*
  - *Caching in name translation*
- Key reference values for system design

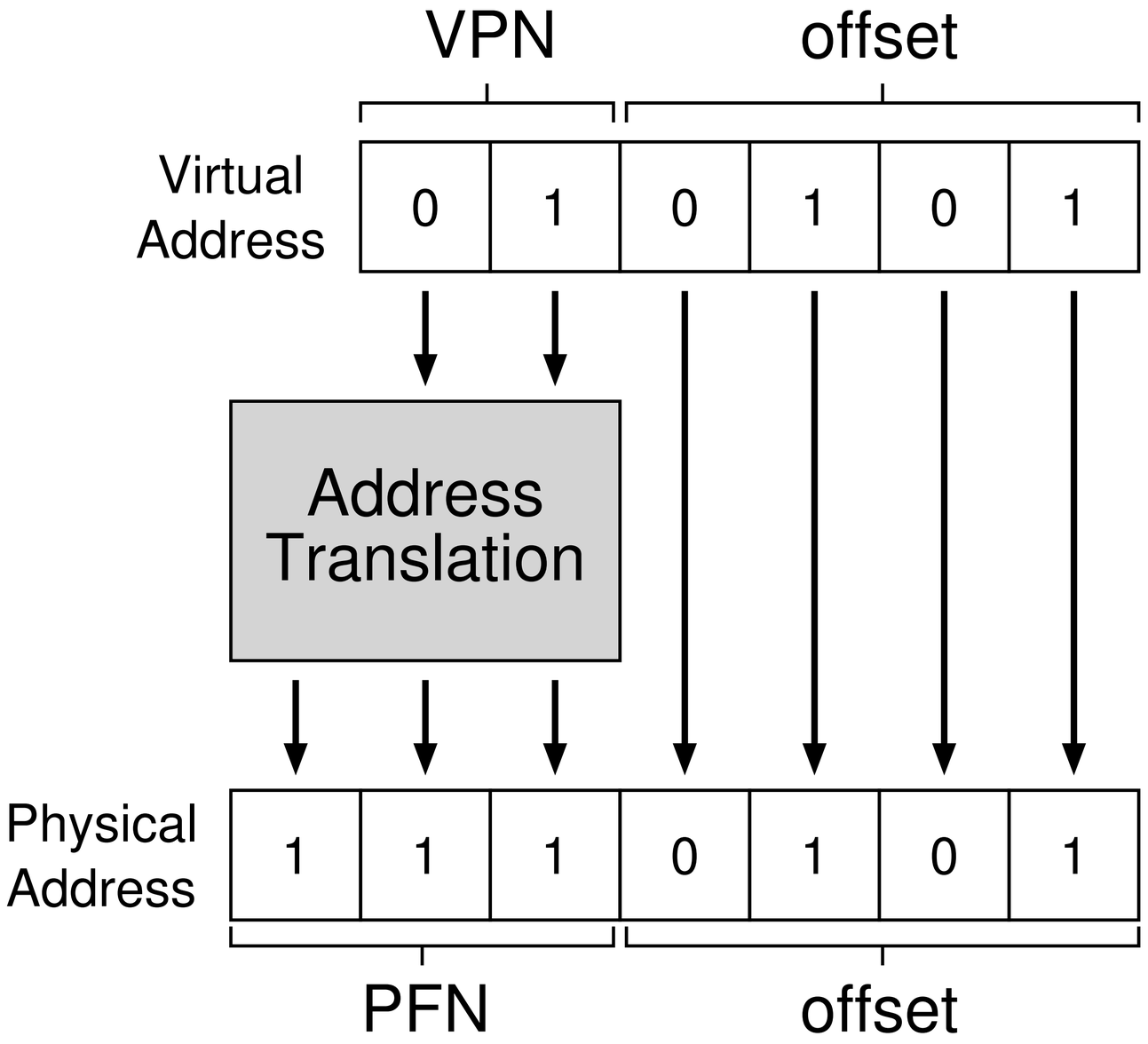
Examples of Names

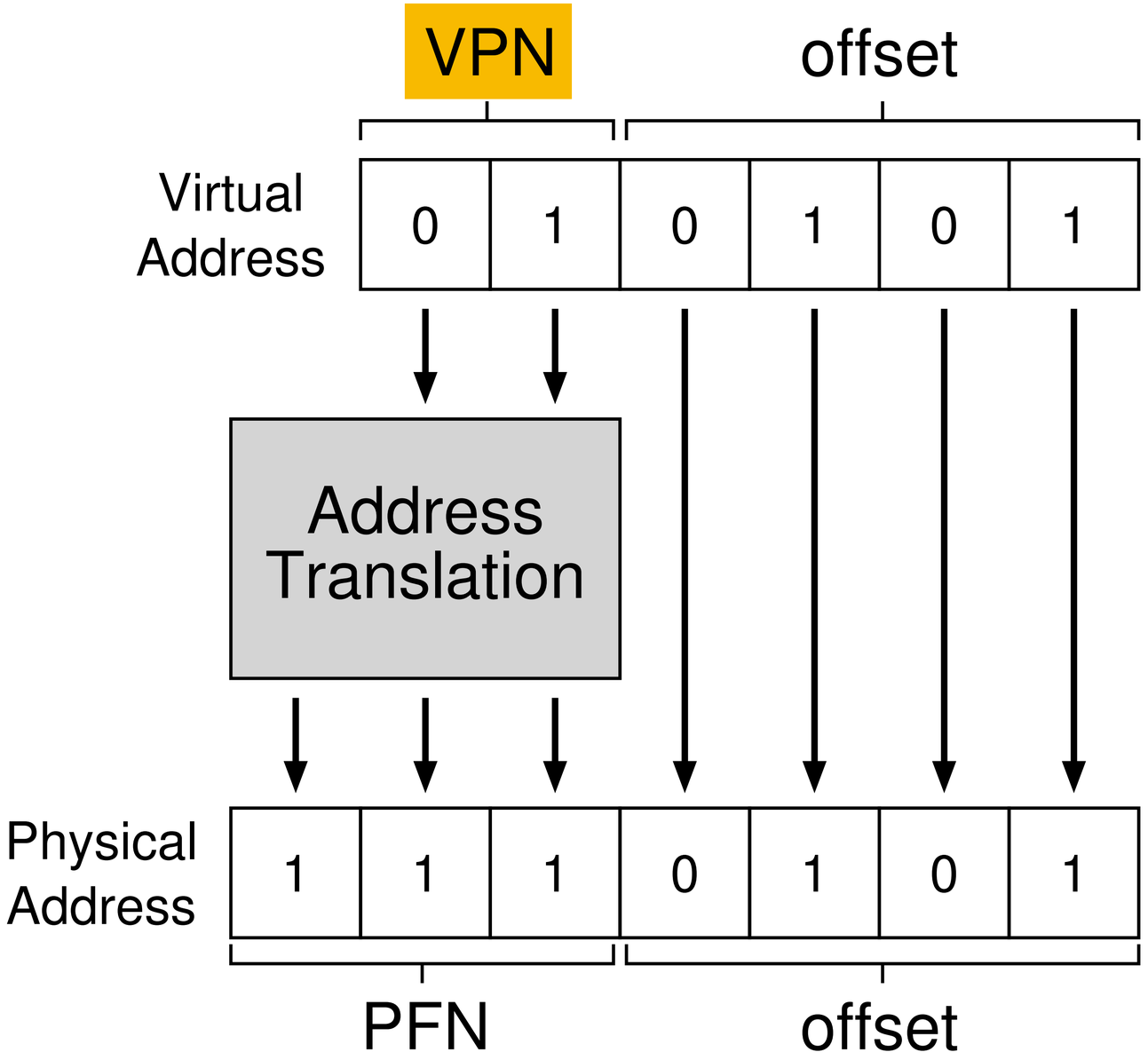
- Memory address
  - *names a memory location*
- Pointer
  - `void*` names the location of a memory word
  - `int*` names the location of an integer
- Virtual memory address
  - *names (from userspace) a physical memory address*

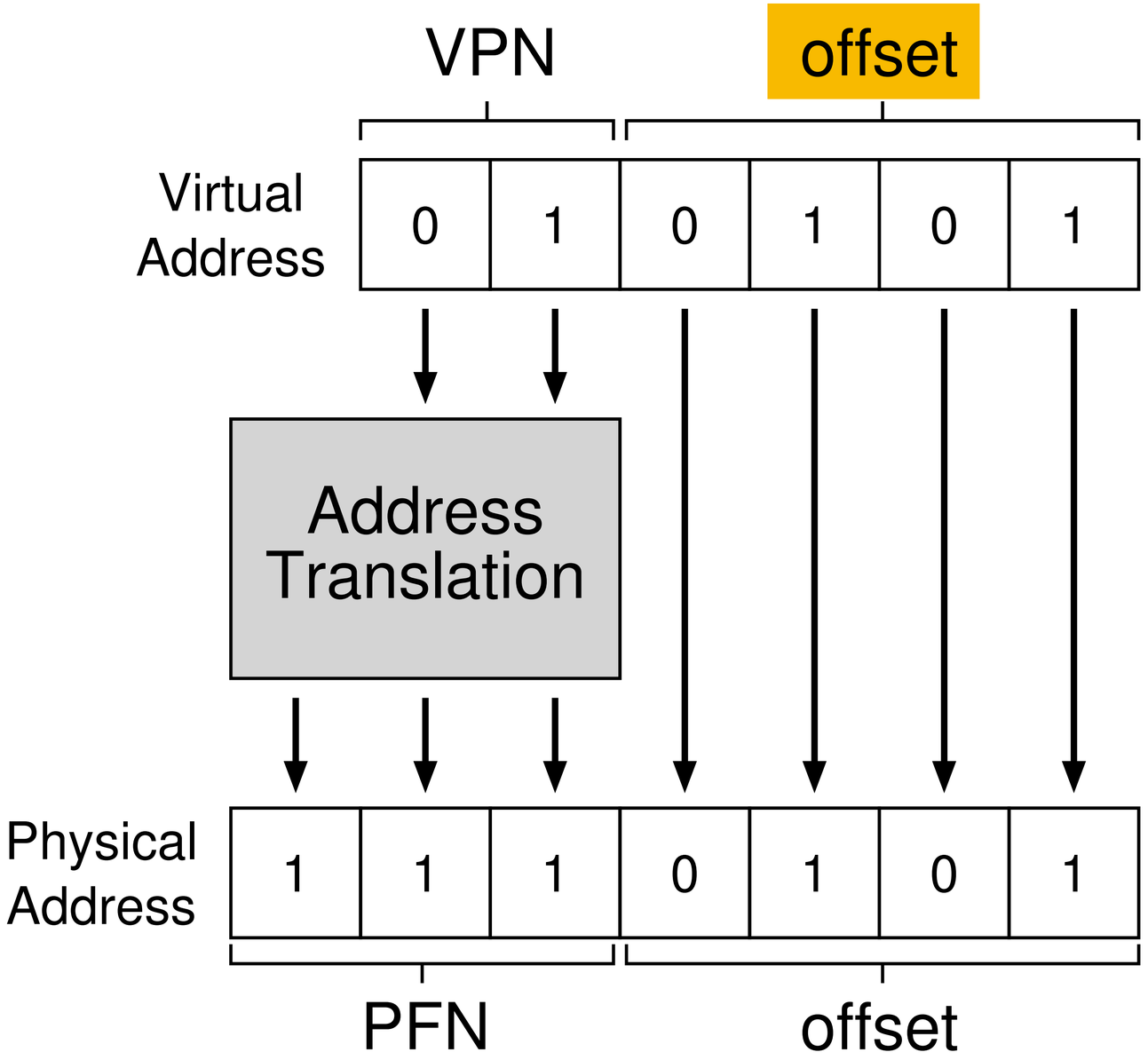
Names & Page Tables

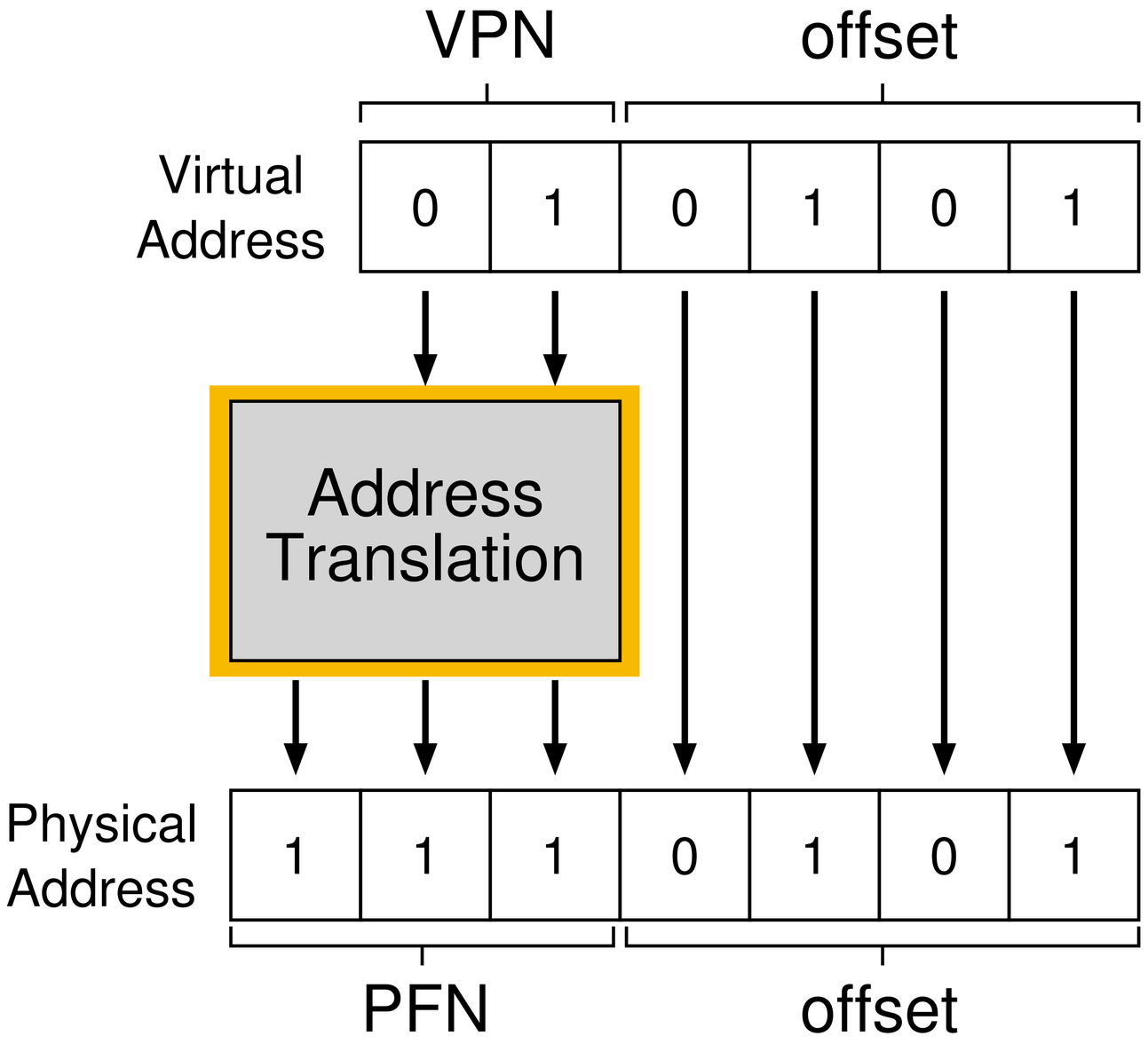
Names

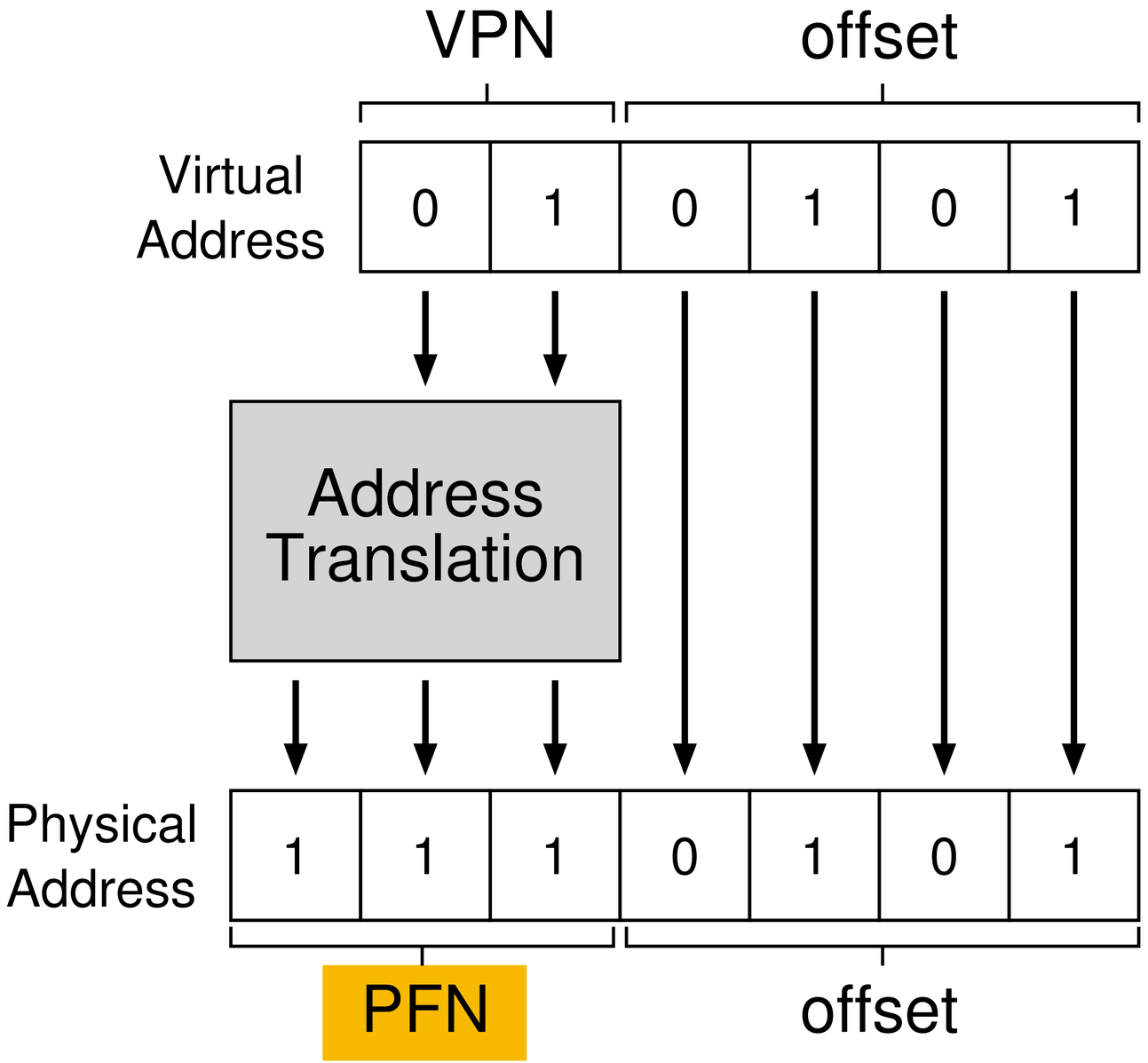
- Scope
  - *Private: unique within a context (e.g., a private IP address)*
  - *Global: unique across contexts (e.g., a global IP address)*
- Structure
  - *Hierarchical: name relationship implies object relationship (e.g., two IP addresses sharing the same prefix)*
  - *Flat: name relationship implies nothing (e.g., content IDs in Peer-to-Peer networks)*
- Naming system
  - *Directories of name→value mappings, support name lookups and updates*

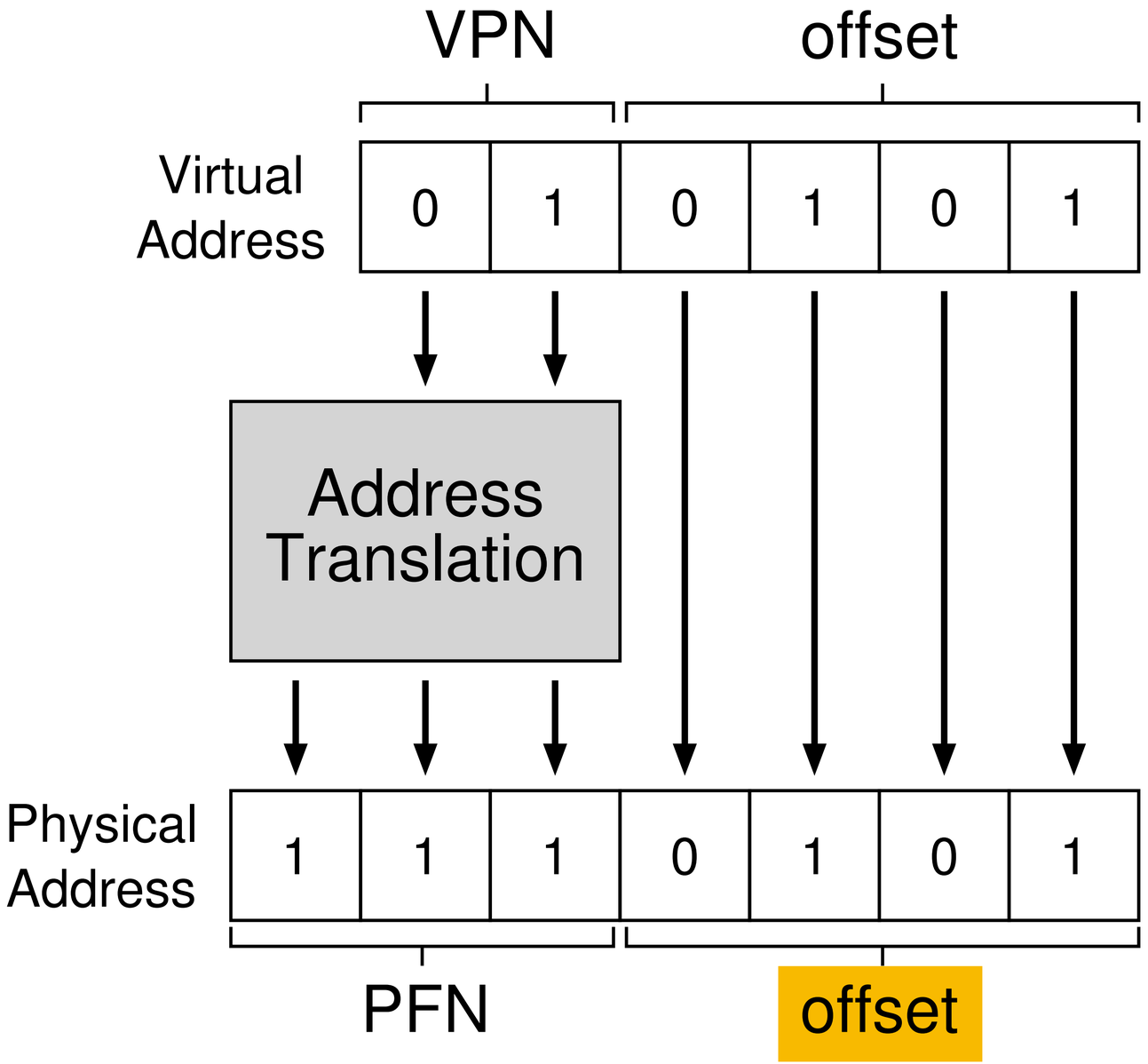


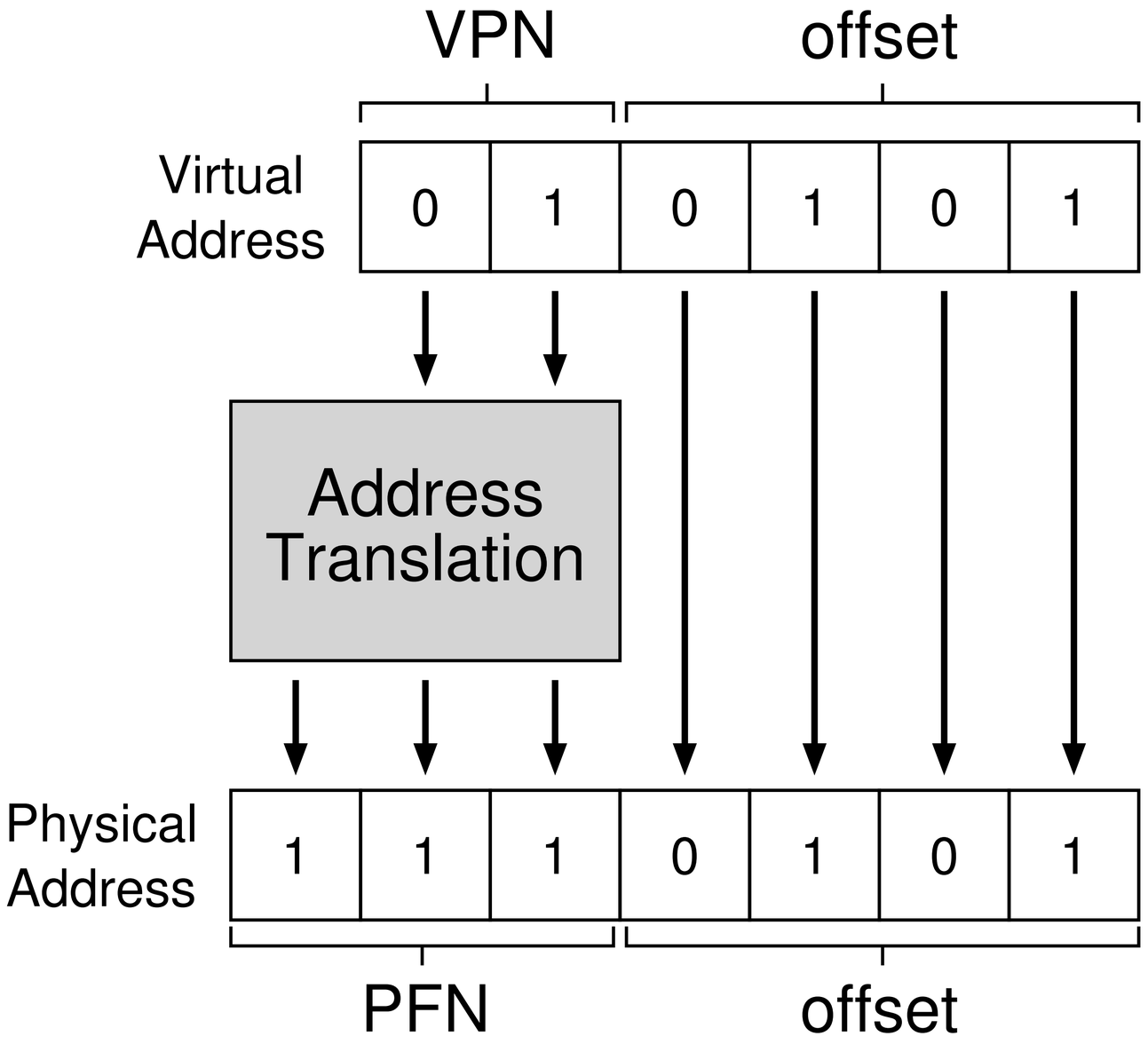




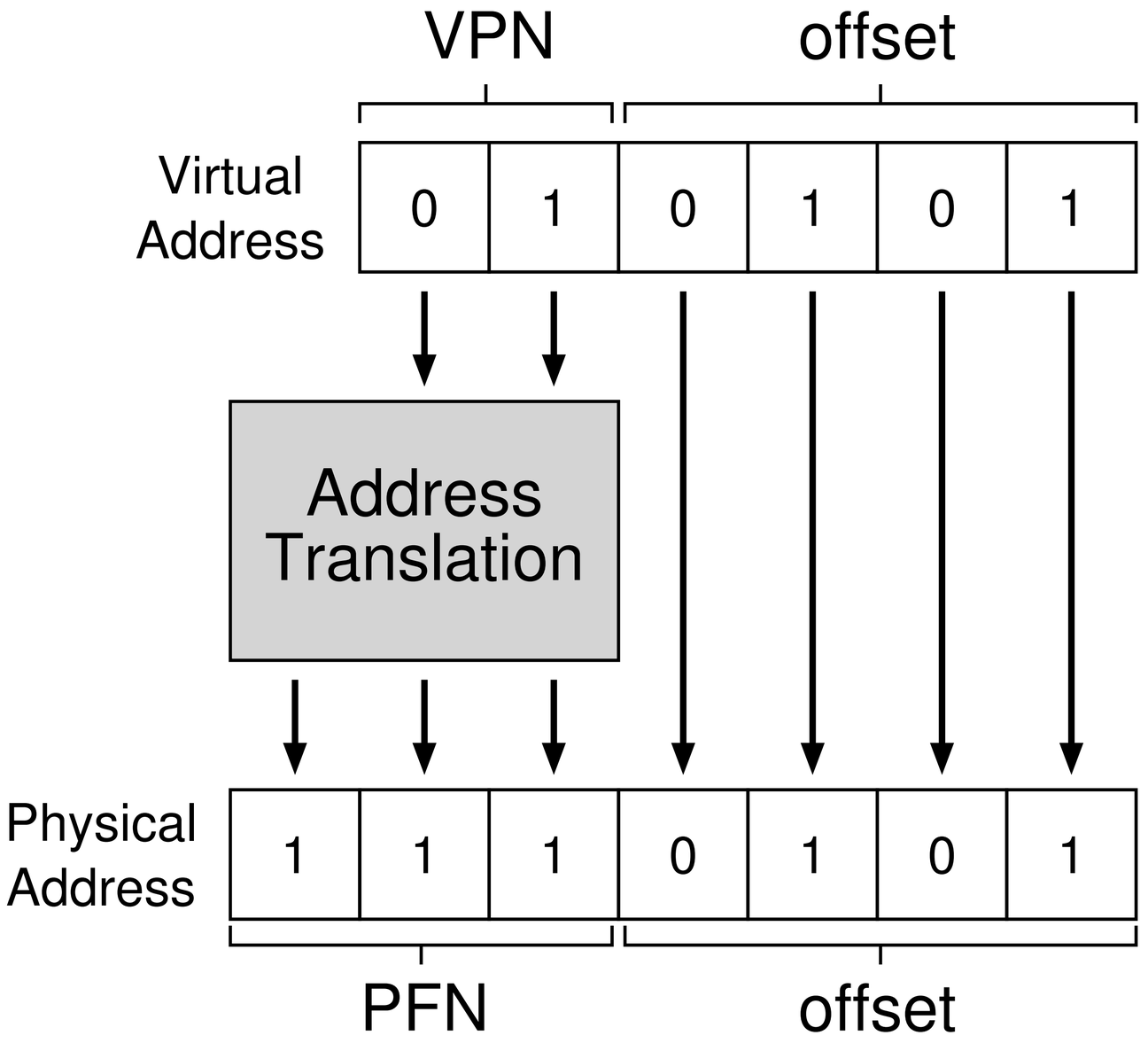








Indirection



Virtual namespace

Name translation controls visibility

"if you can't name it, you can't use it"

Physical namespace

Diagram courtesy of http://pages.cs.wisc.edu/~remzi/OSTEP


INTEL® CORE™ i7
i7-6700K
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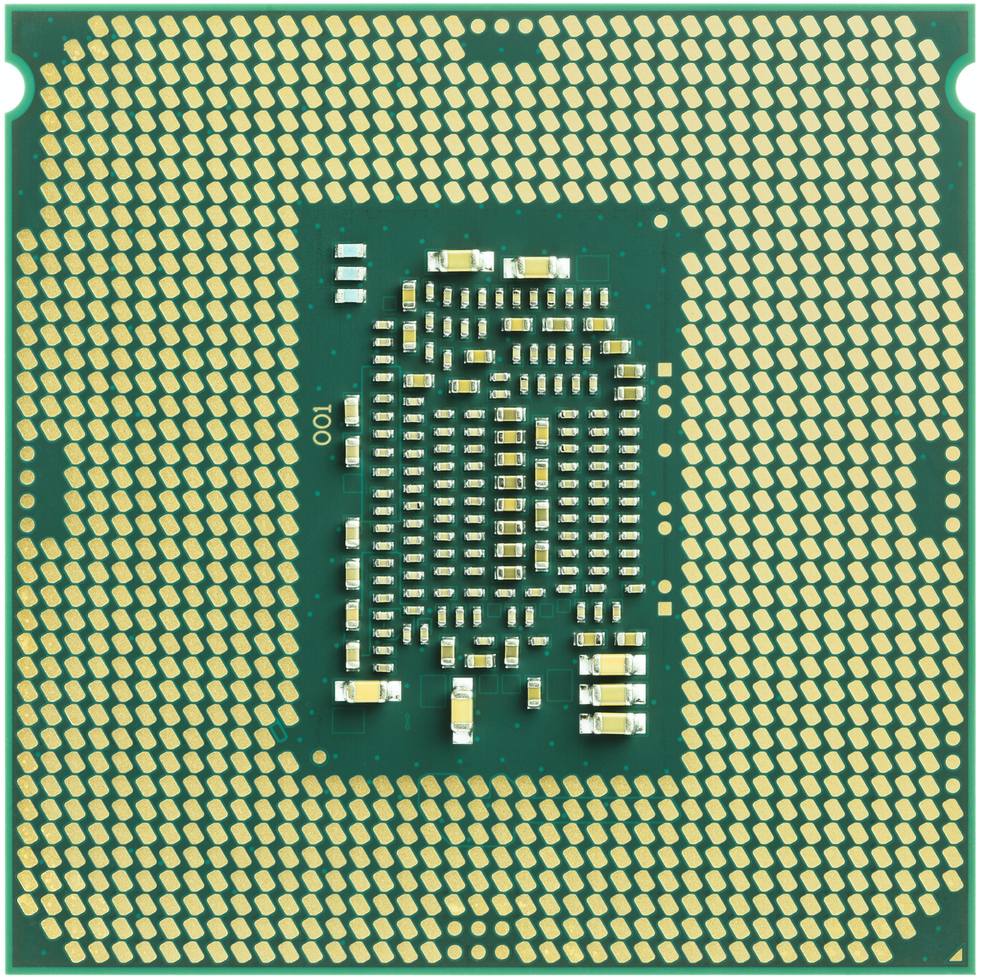
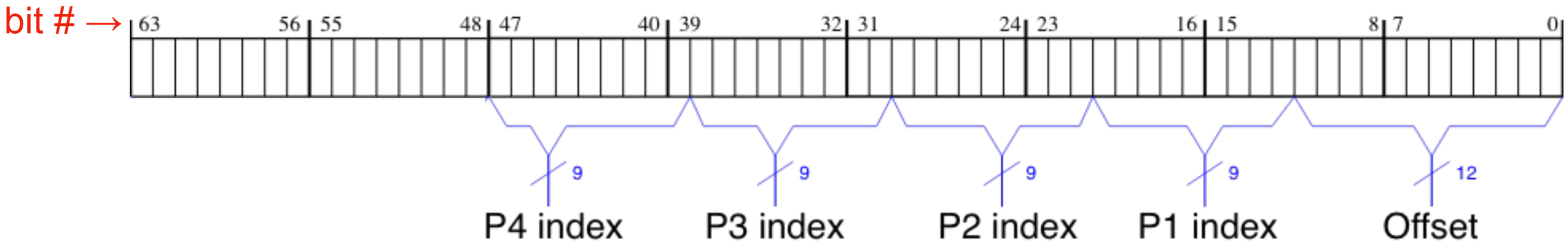
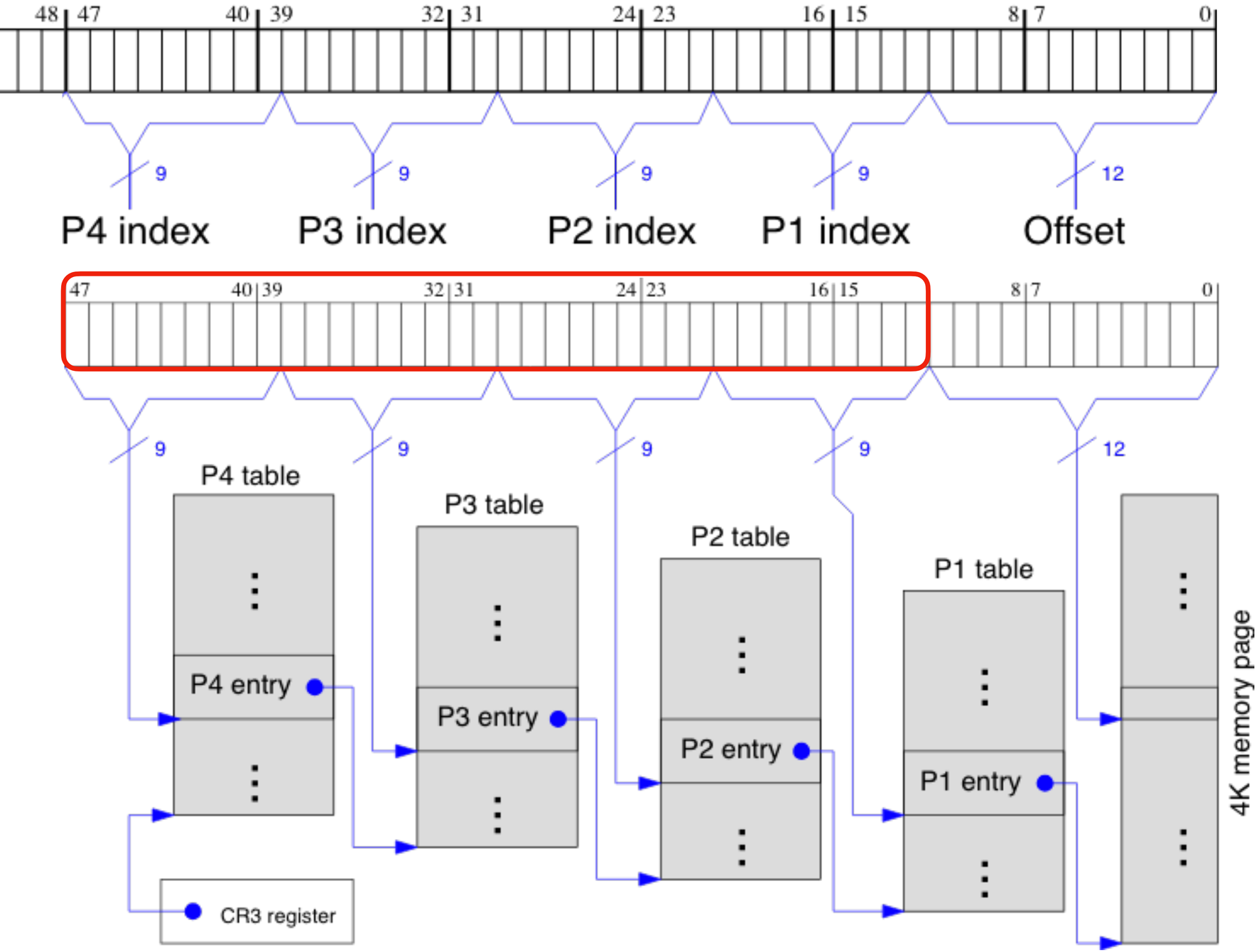




HW walks page tables
OS updates them



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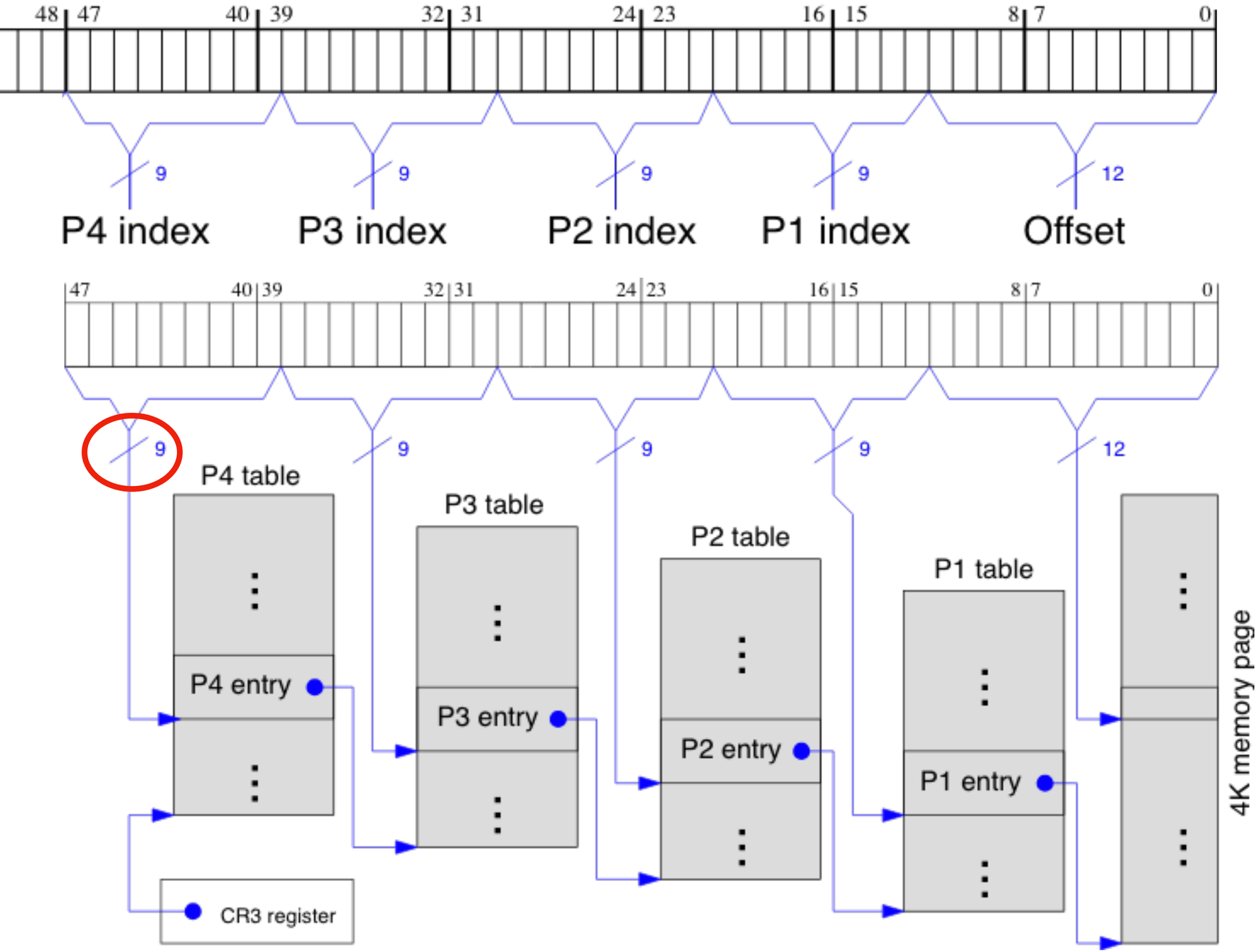

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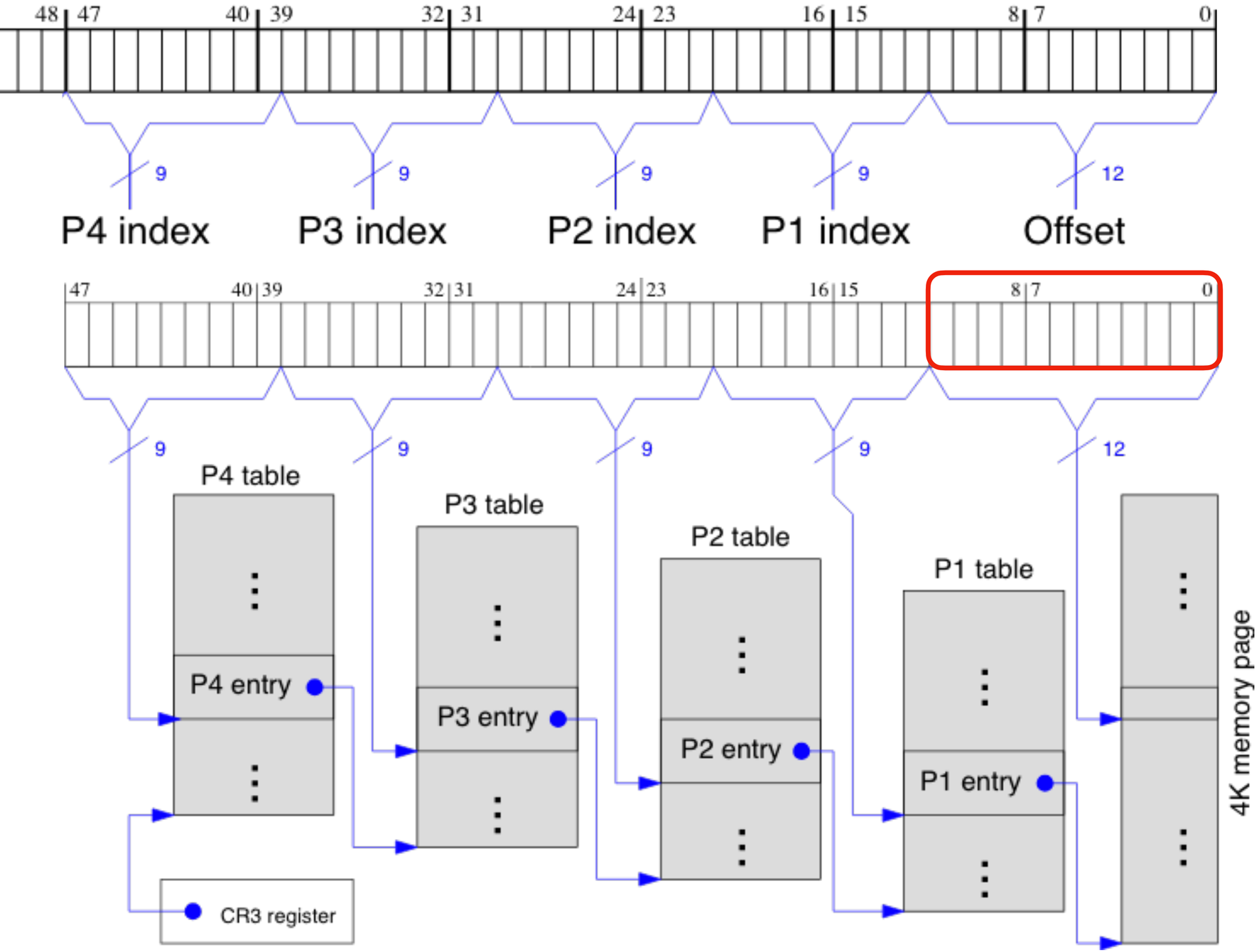

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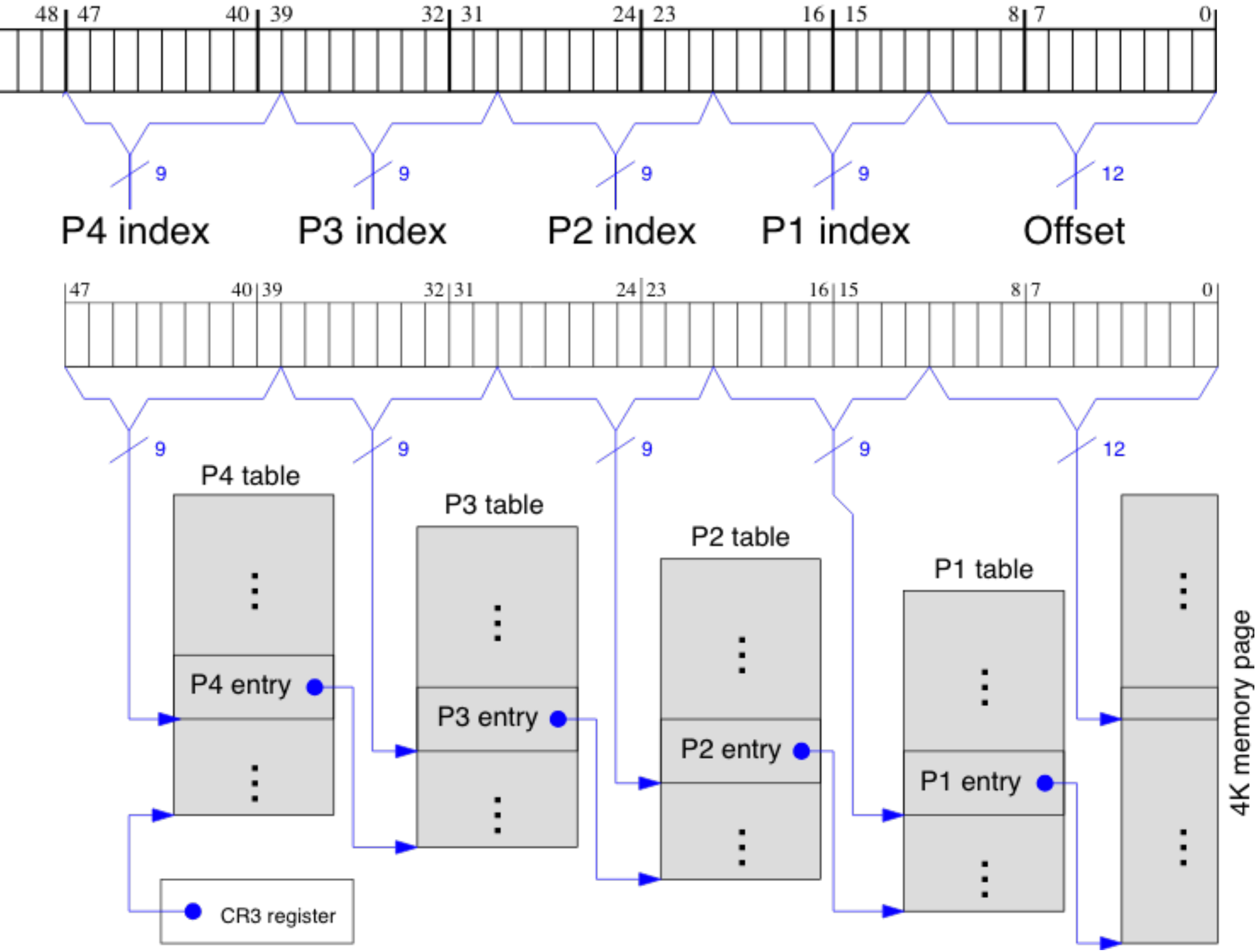

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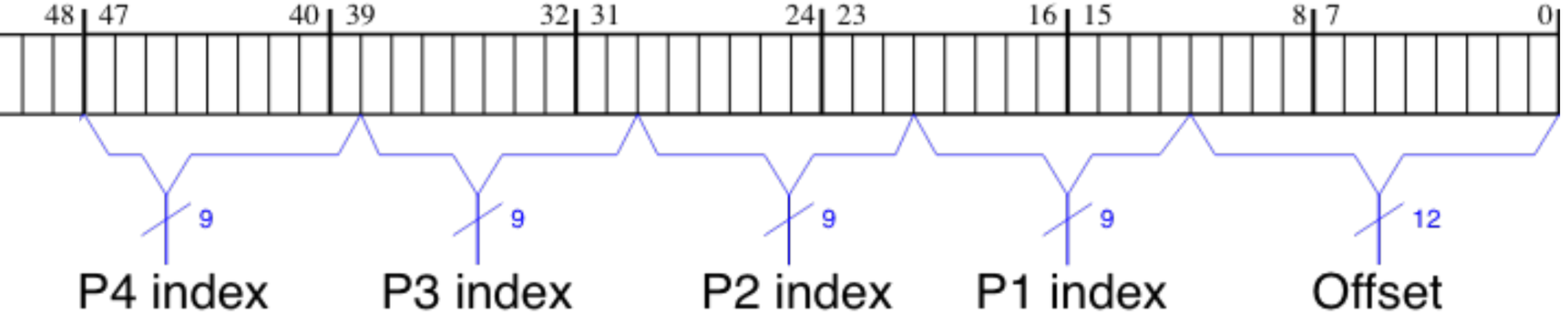

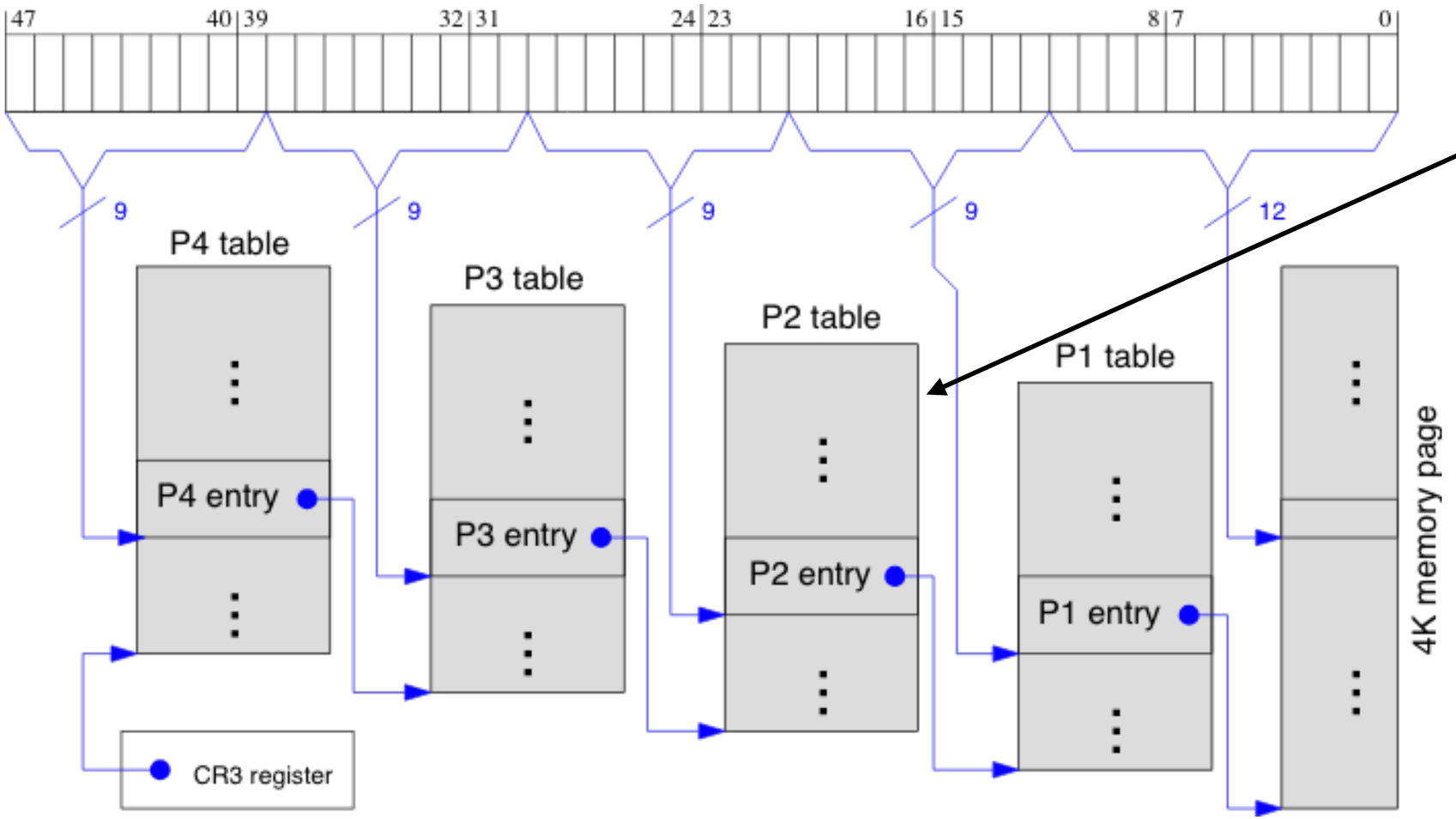

2^9=512 entries
8 bytes / entry

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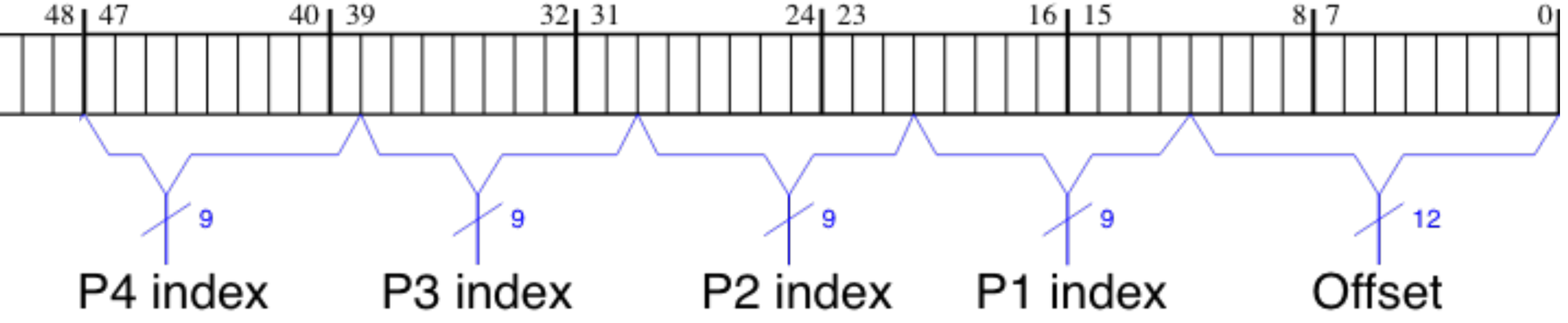

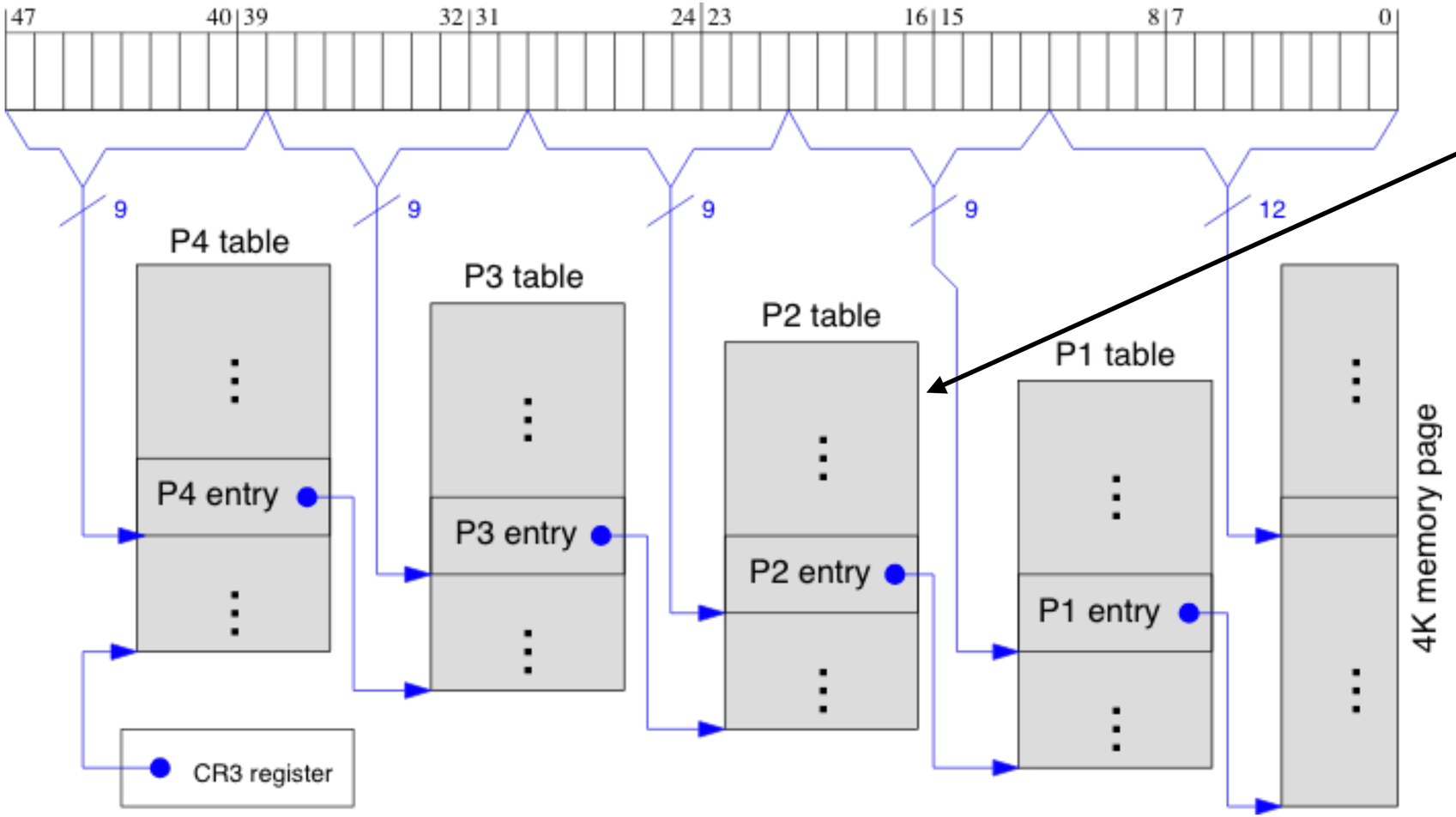

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Hierarchy *of name directories:*
- *scalability for sparse namespaces*
- *locality of reference*

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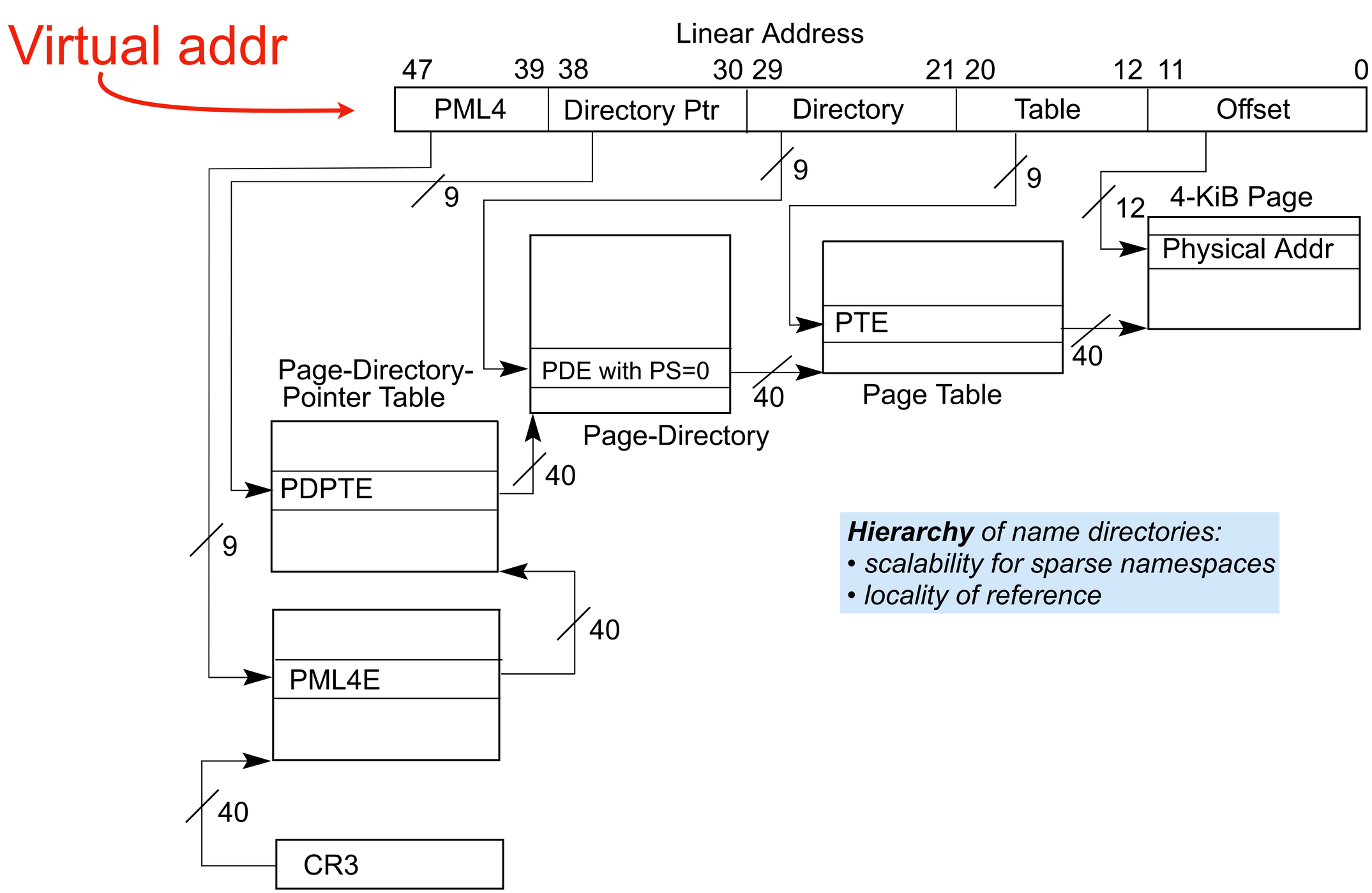
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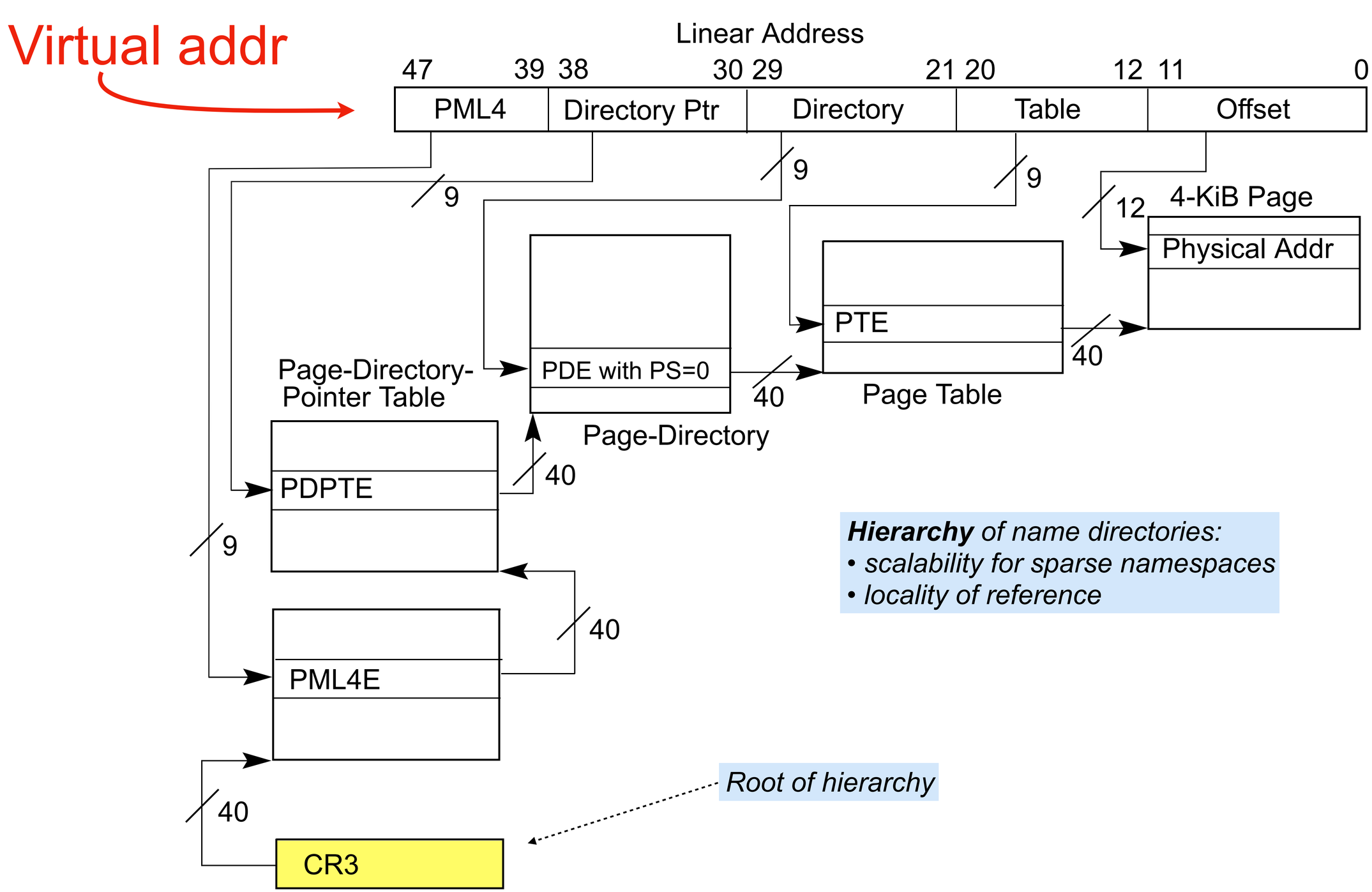
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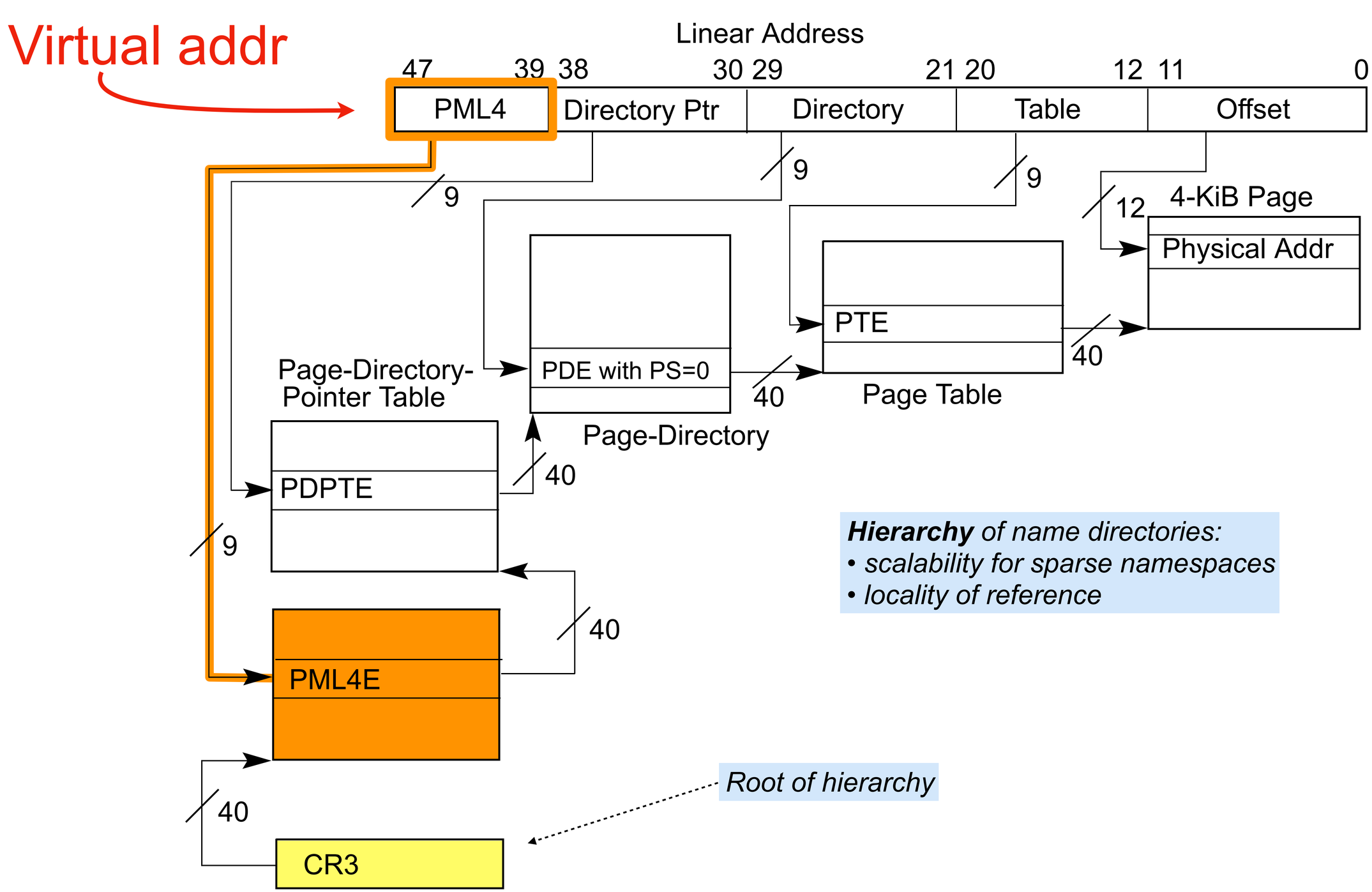
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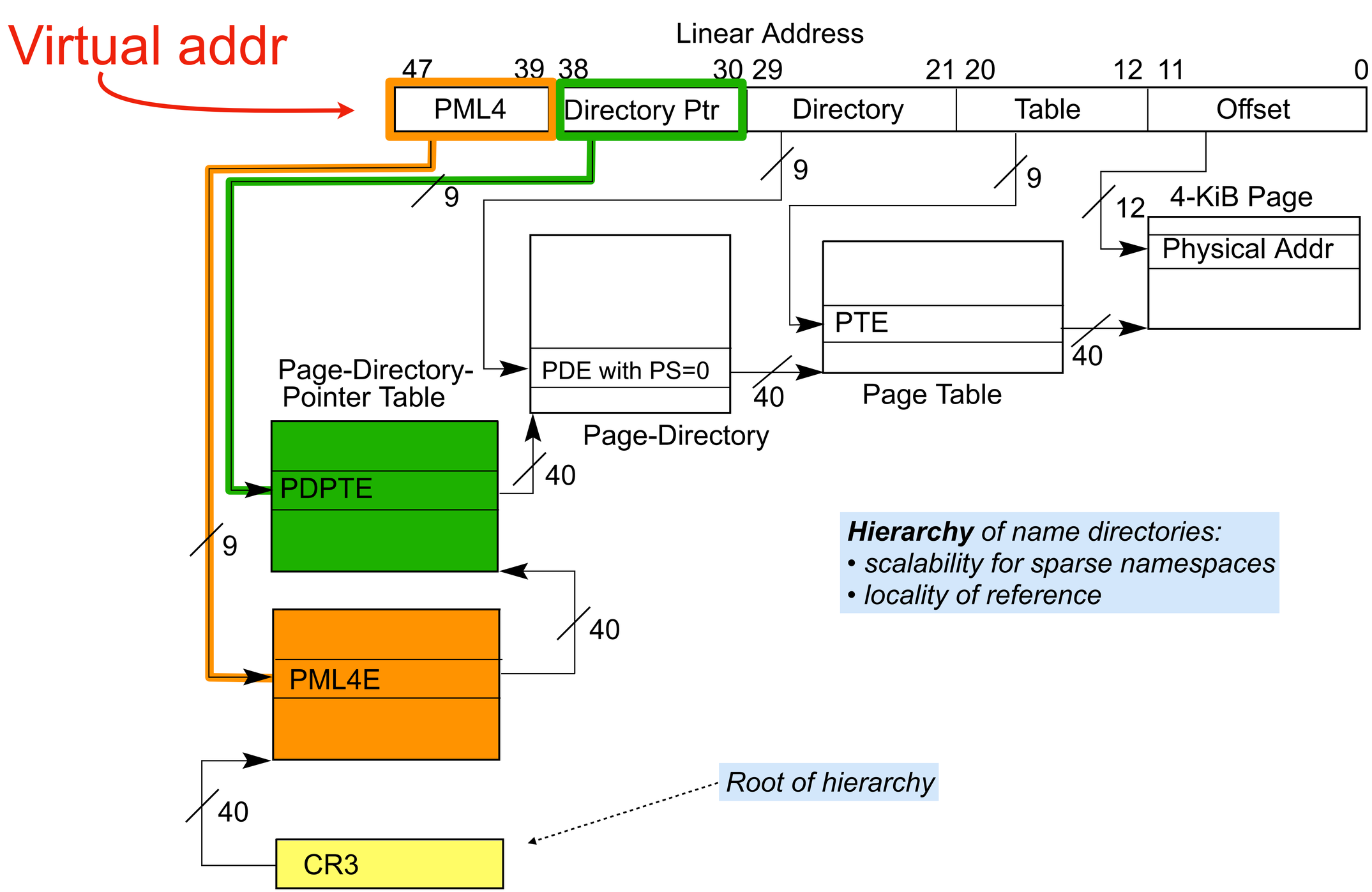
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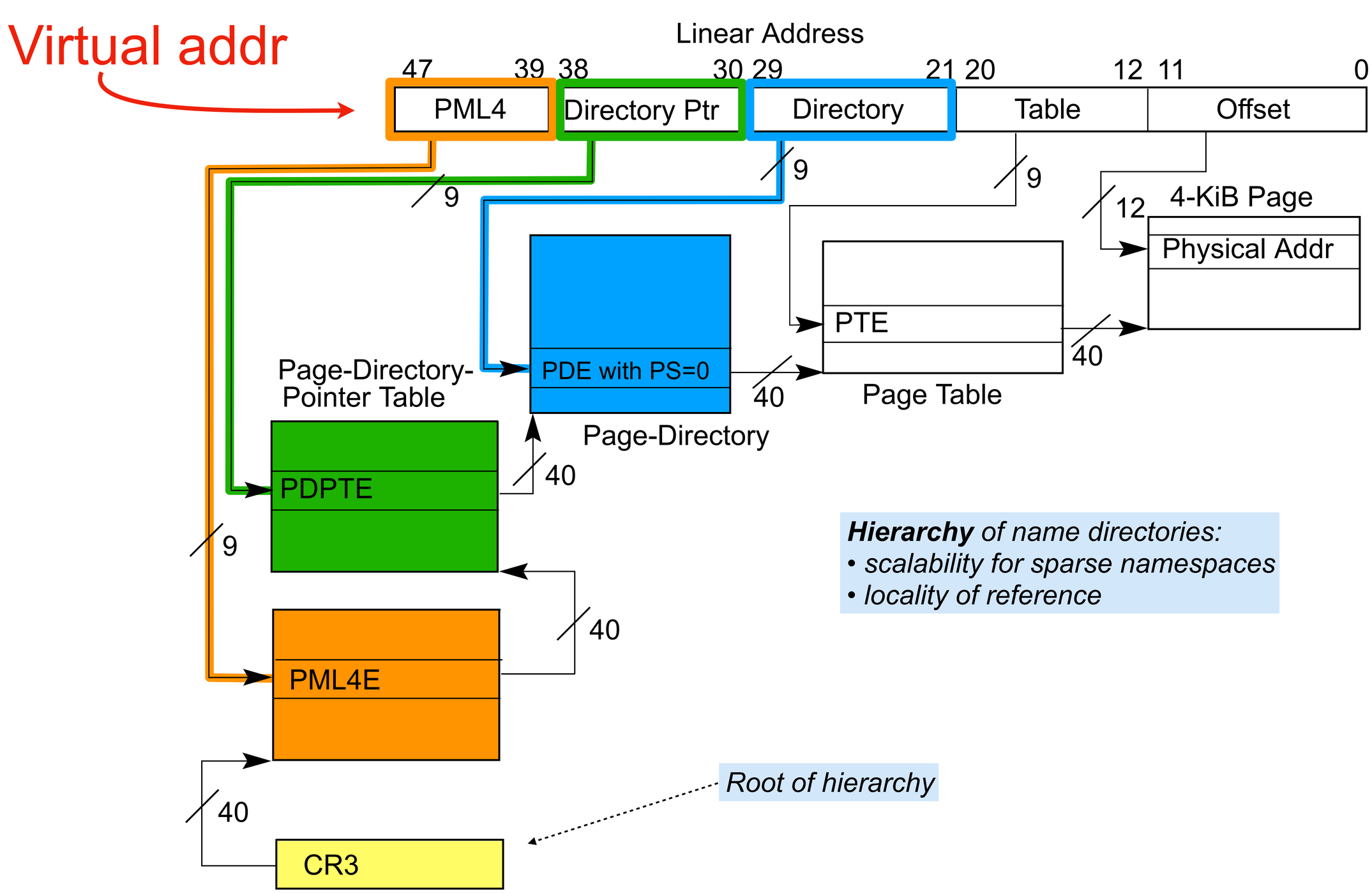
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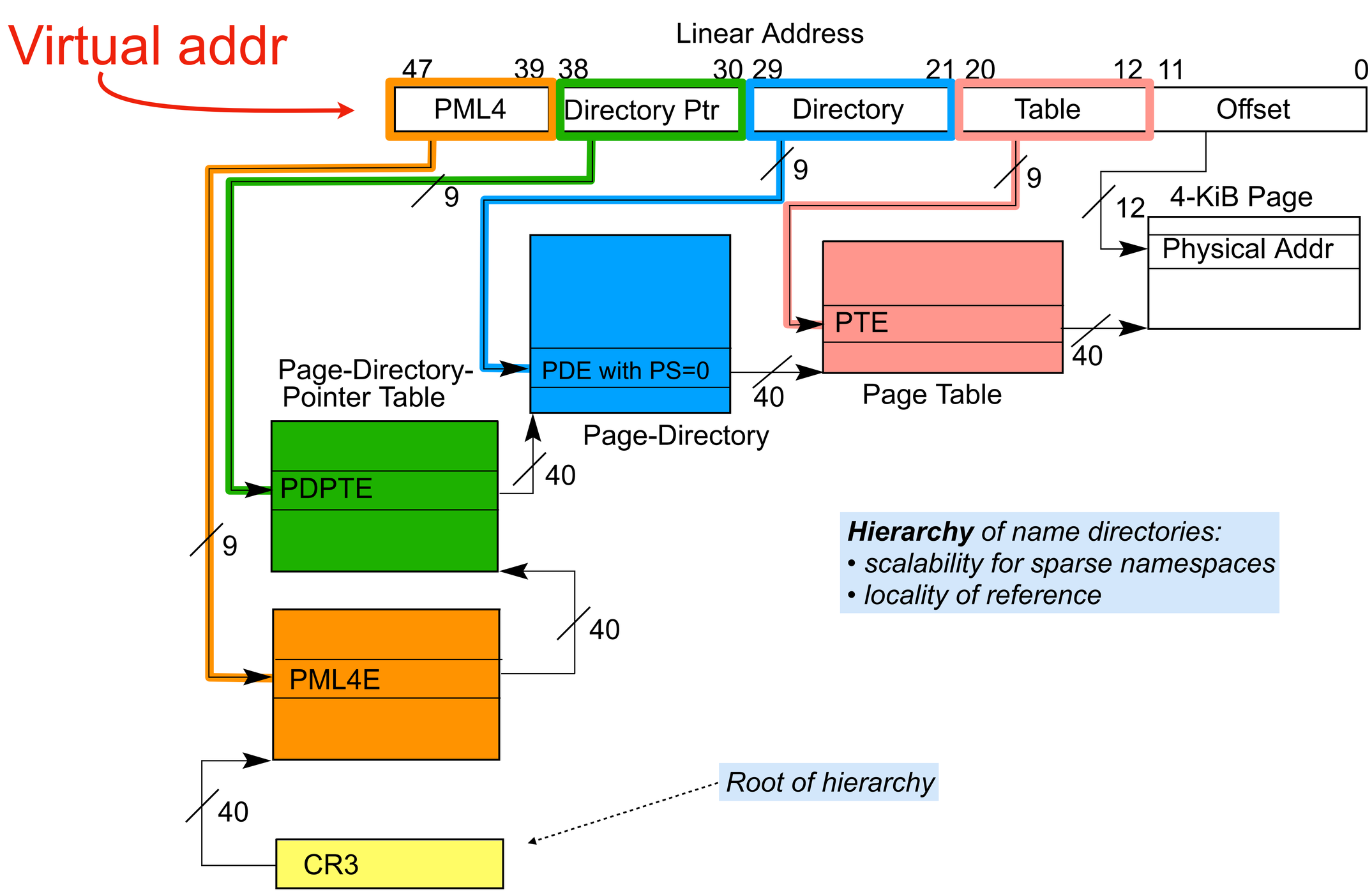
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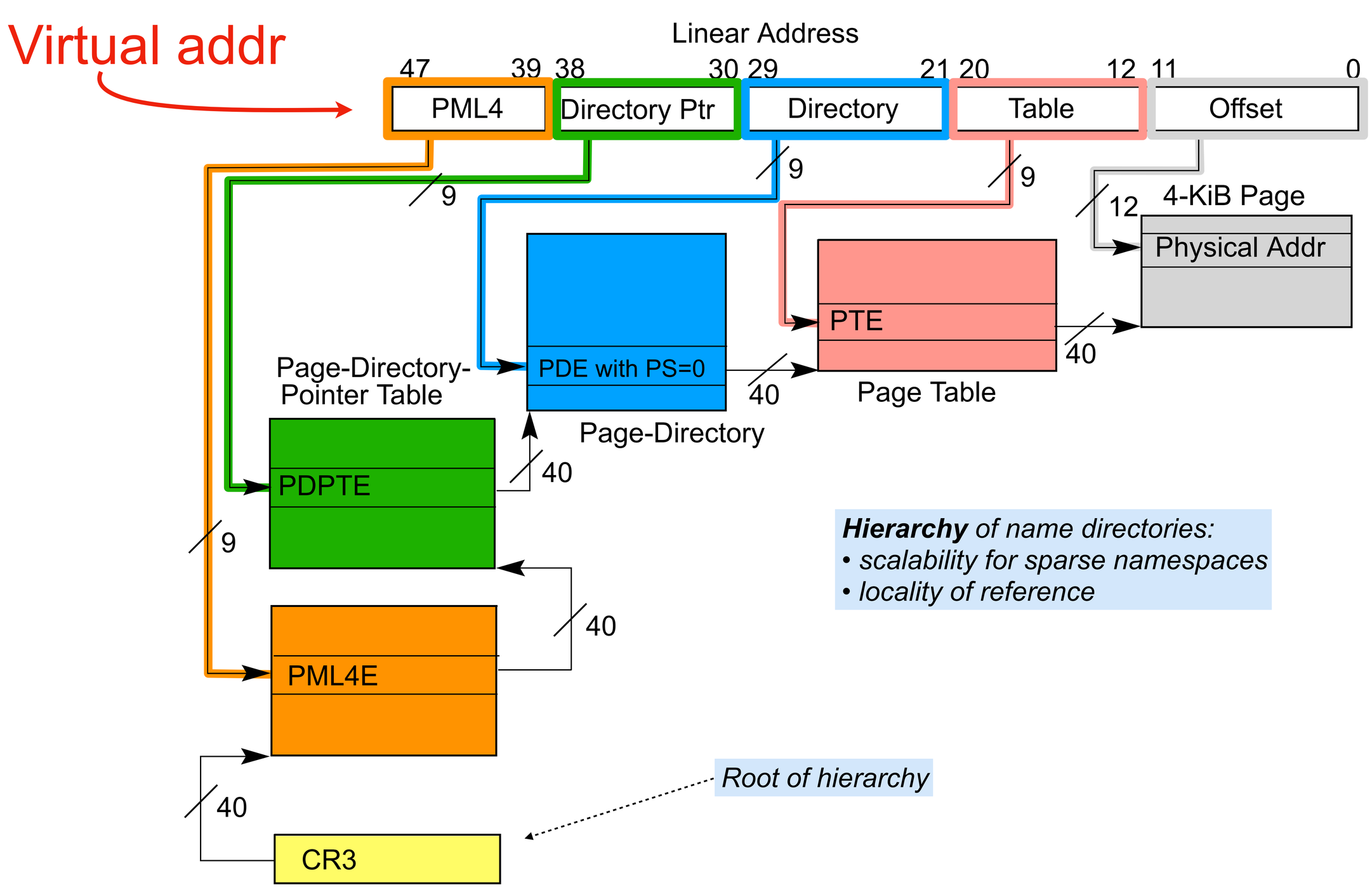
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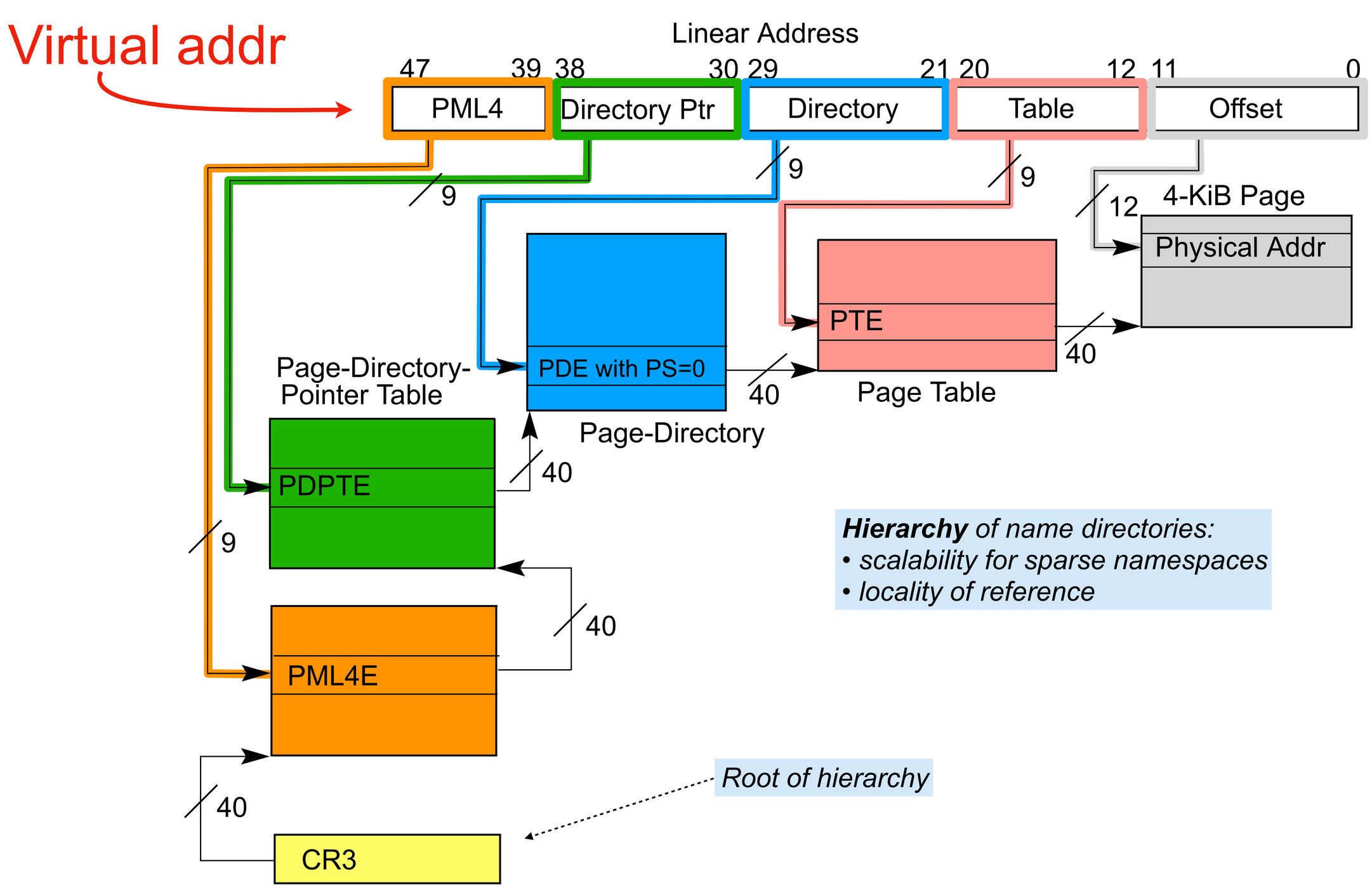
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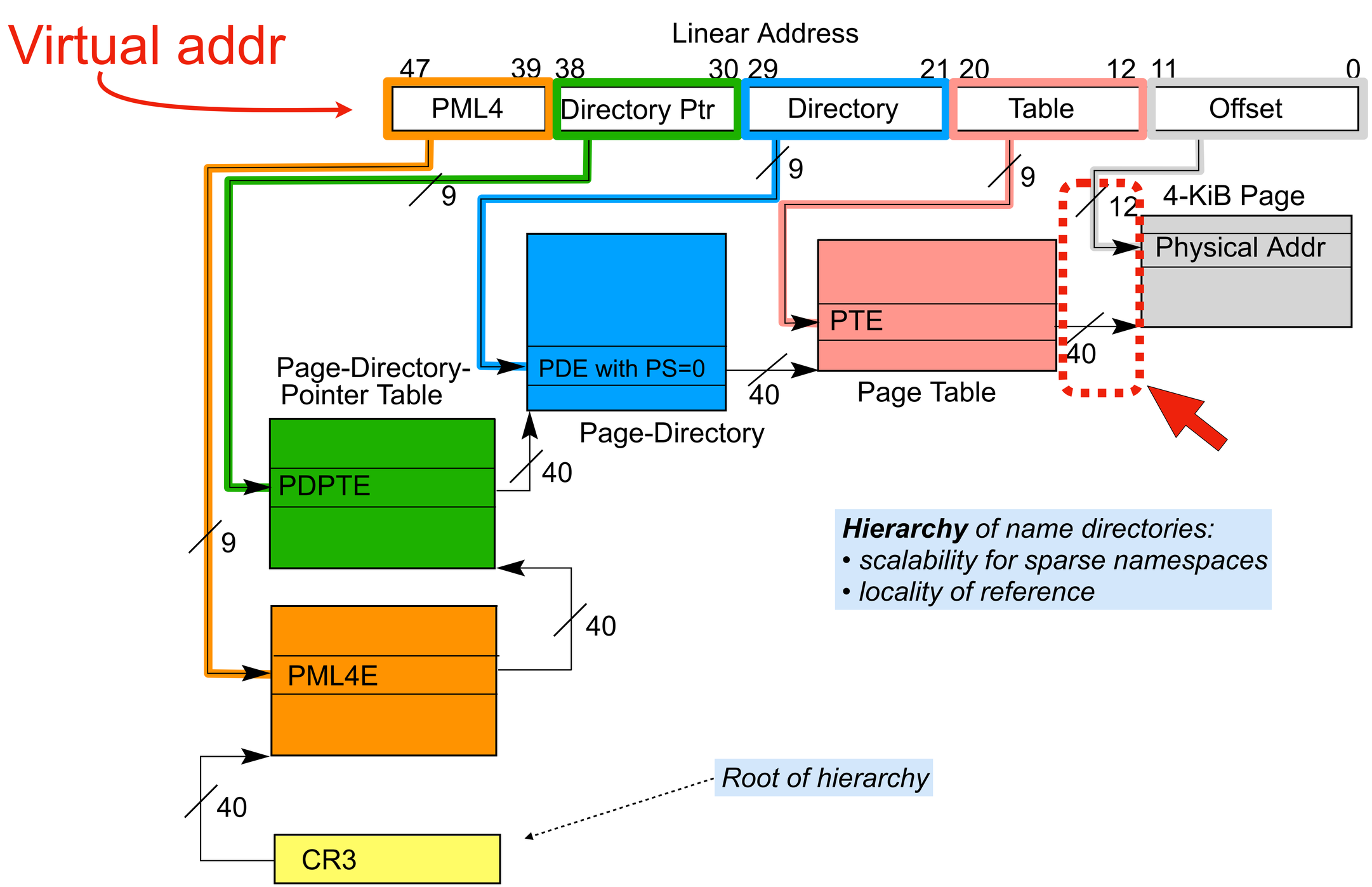
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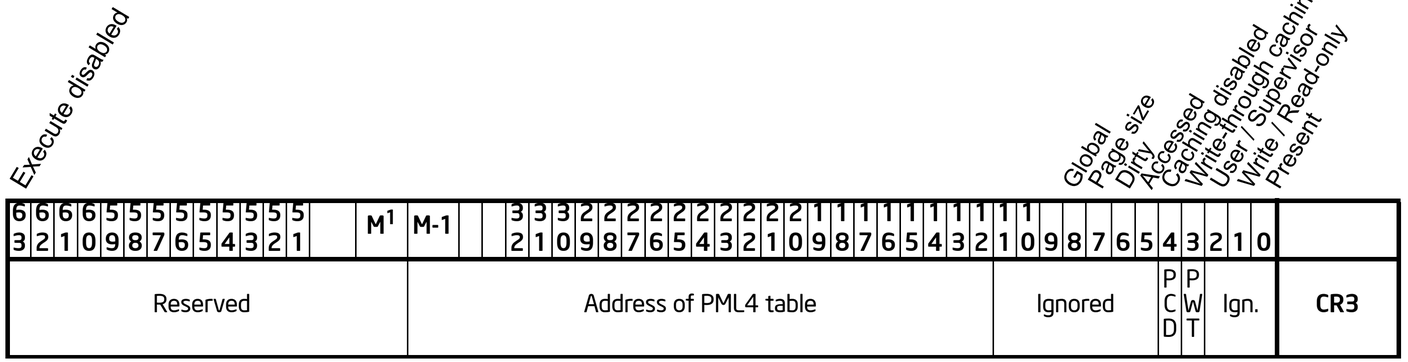

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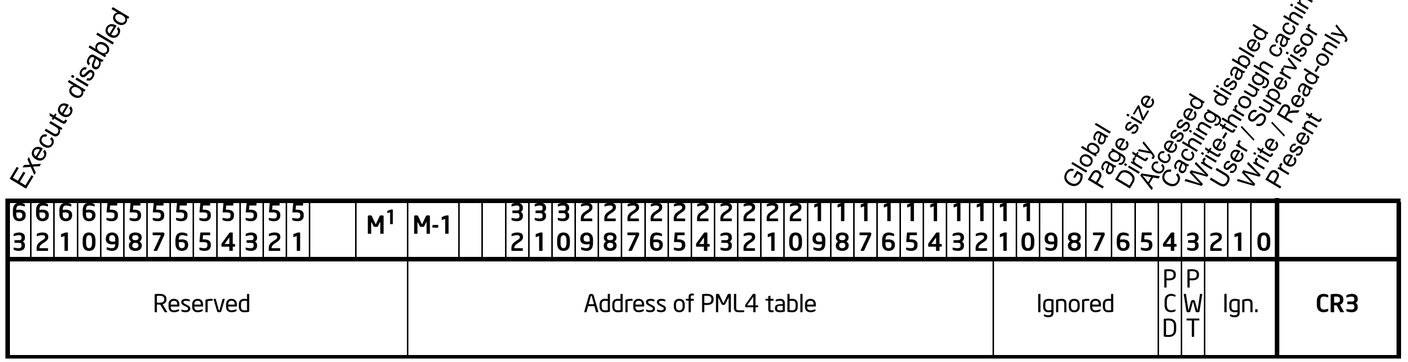

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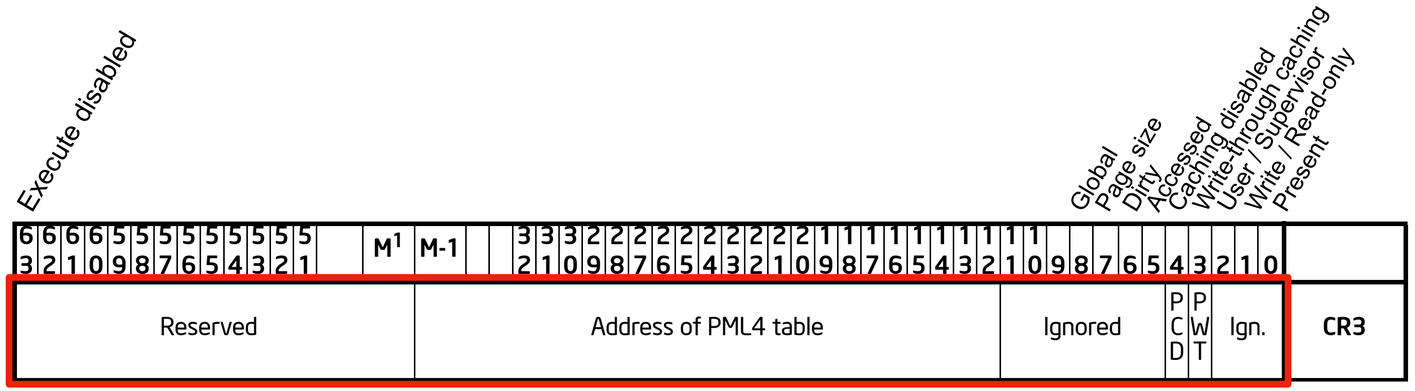

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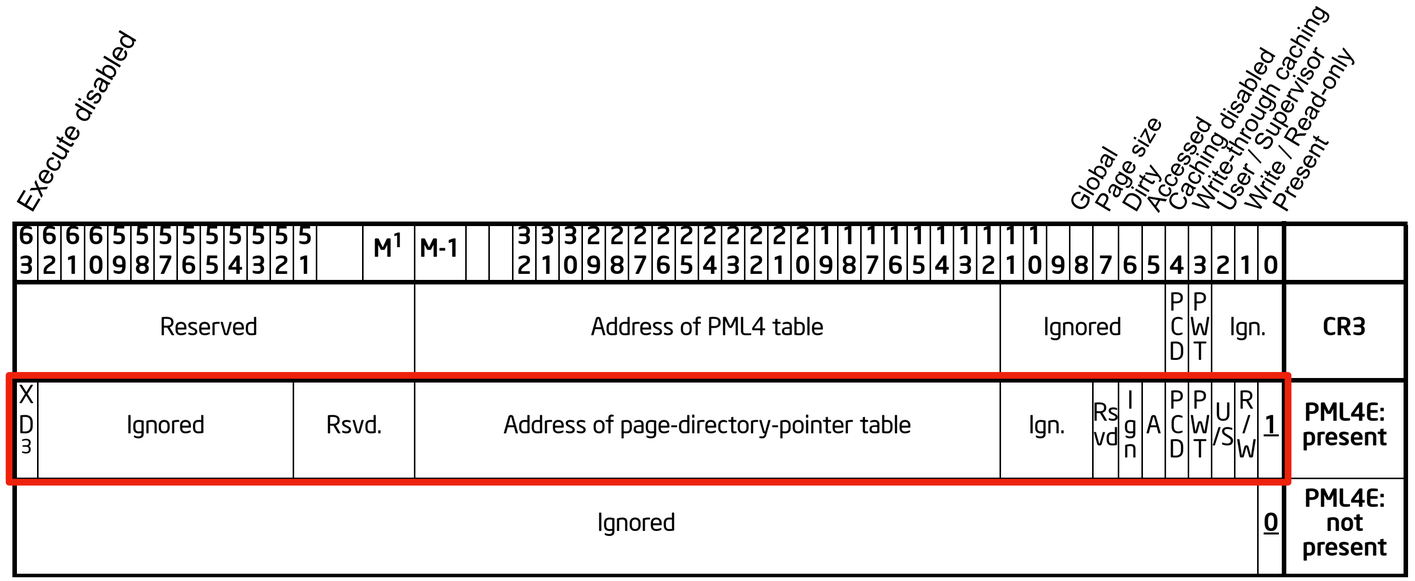

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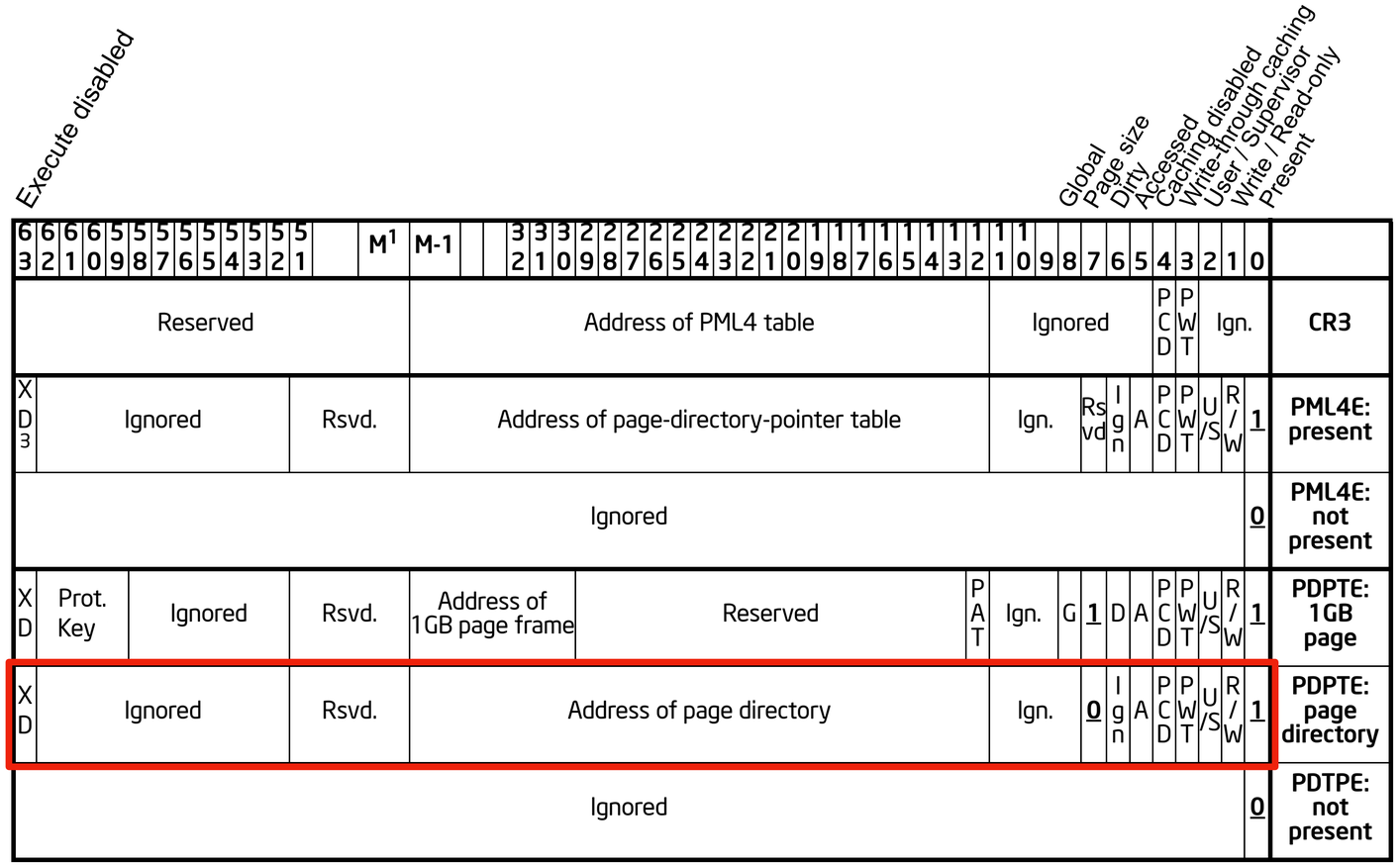

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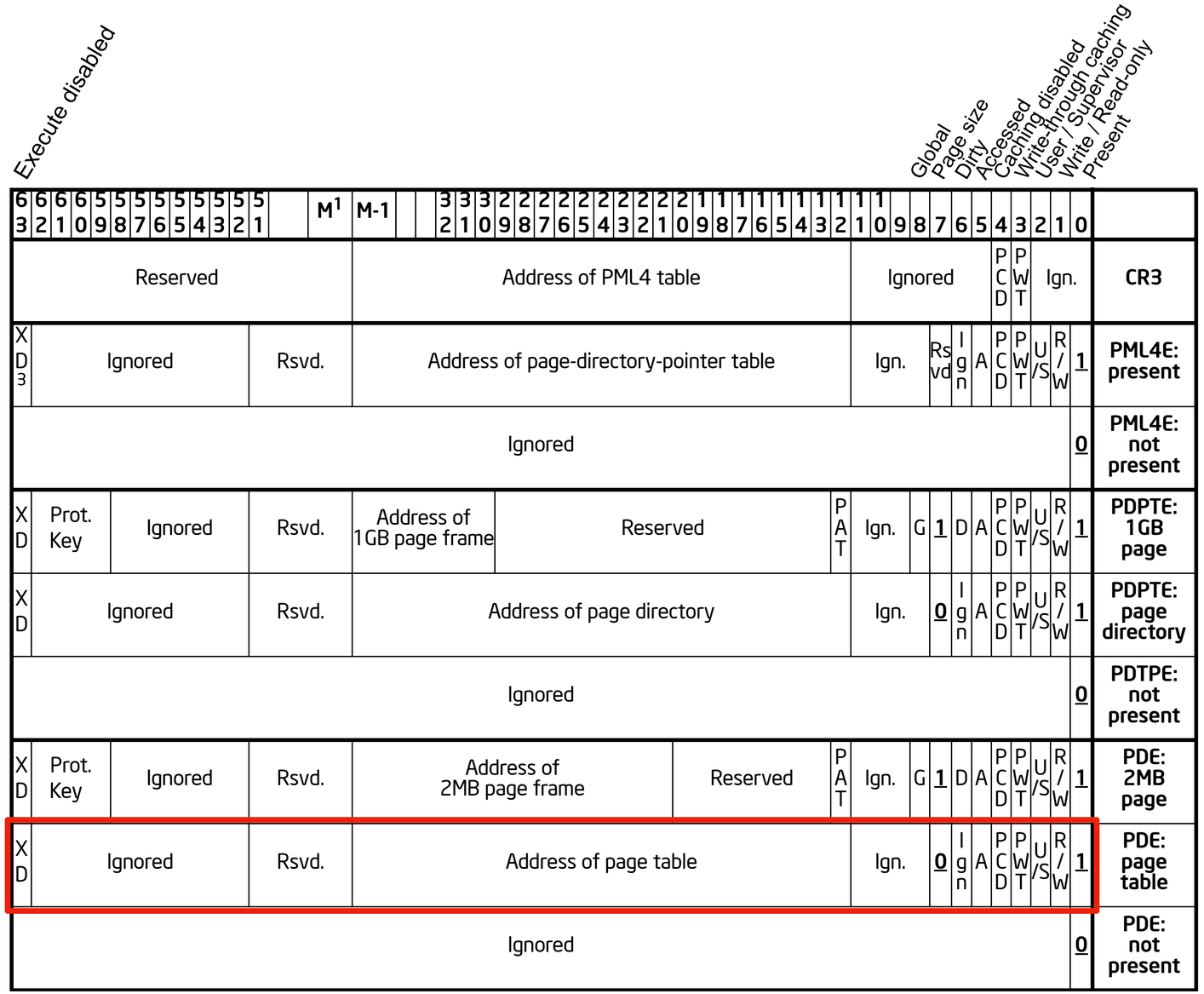

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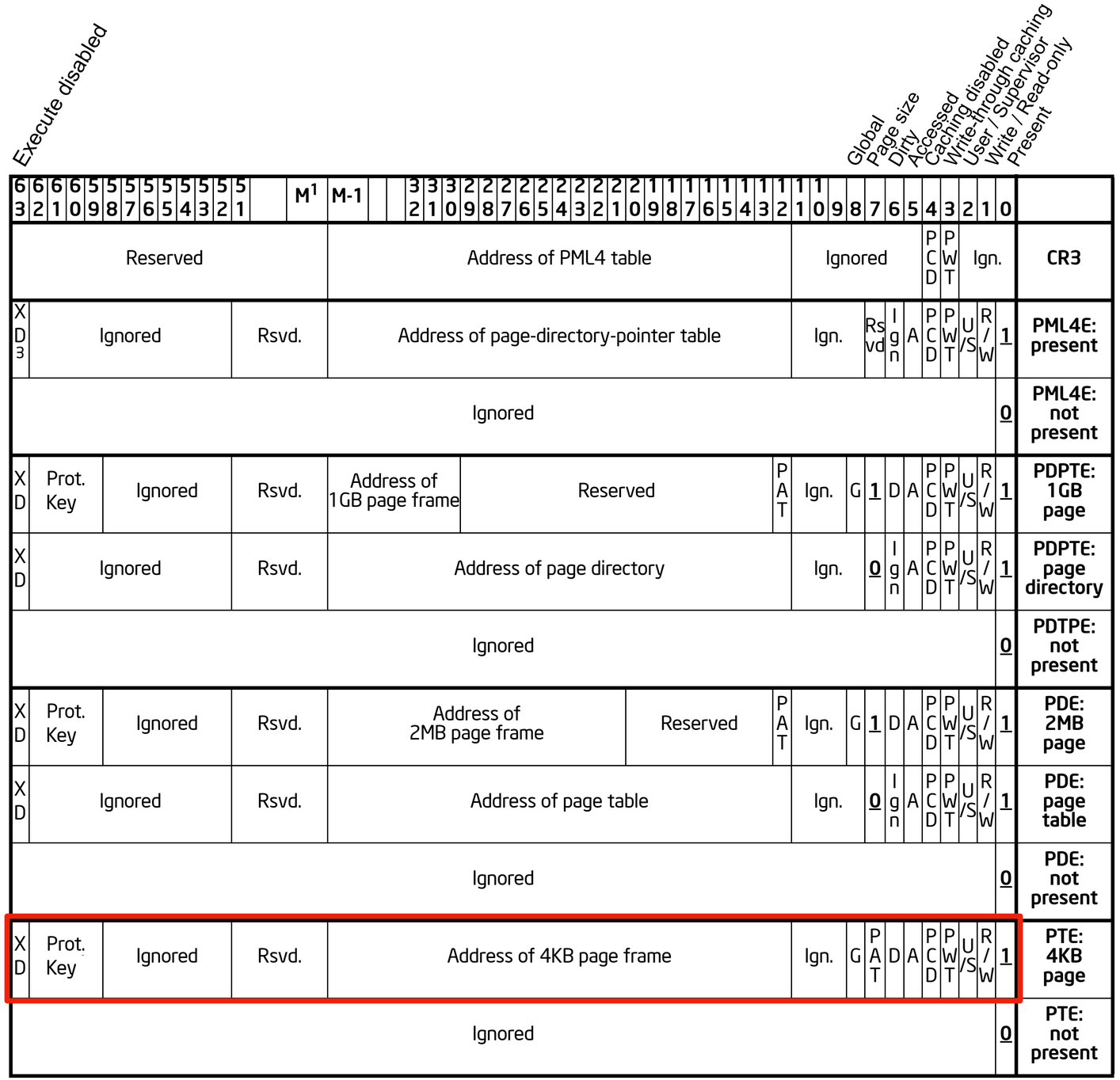

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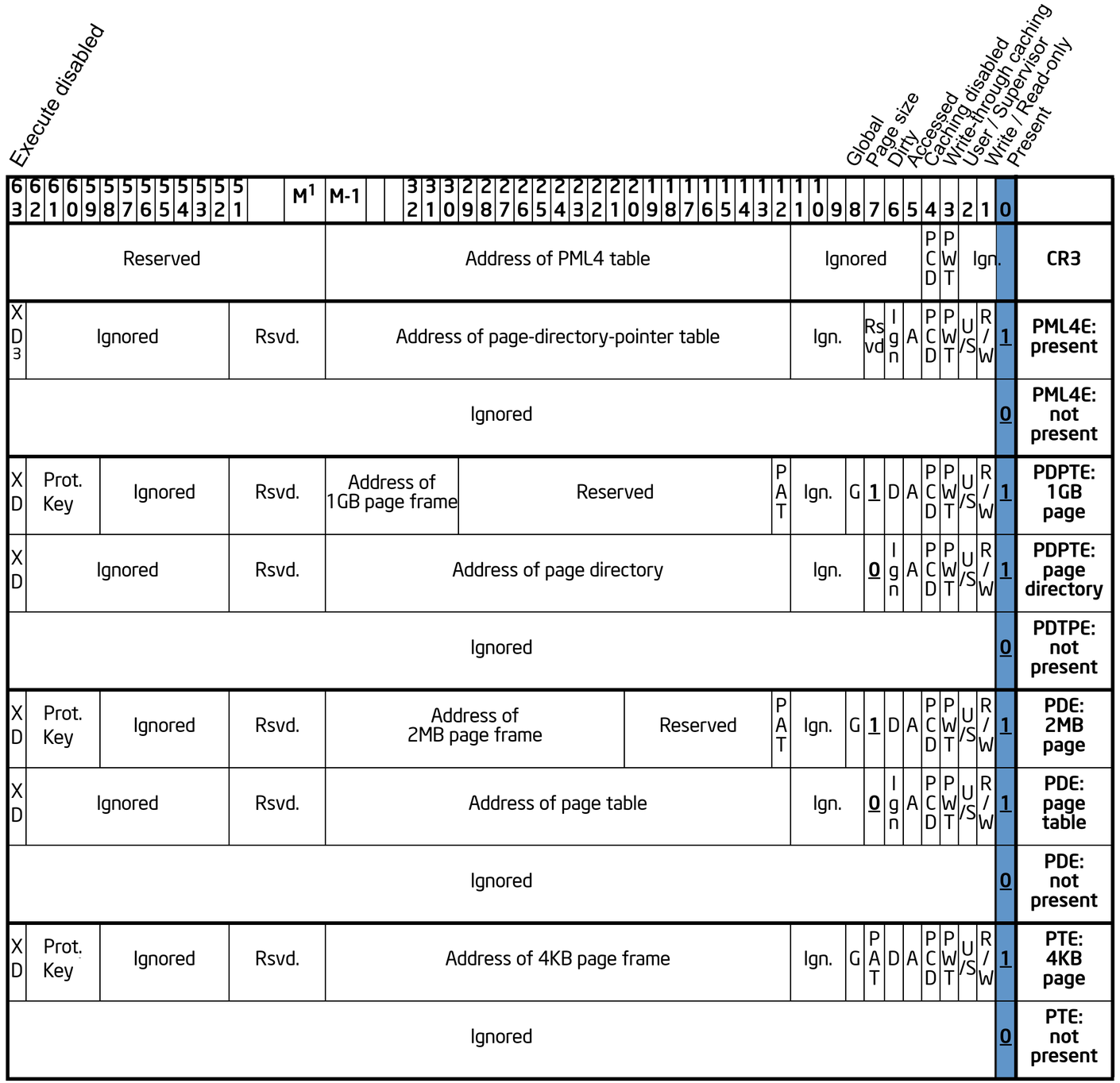

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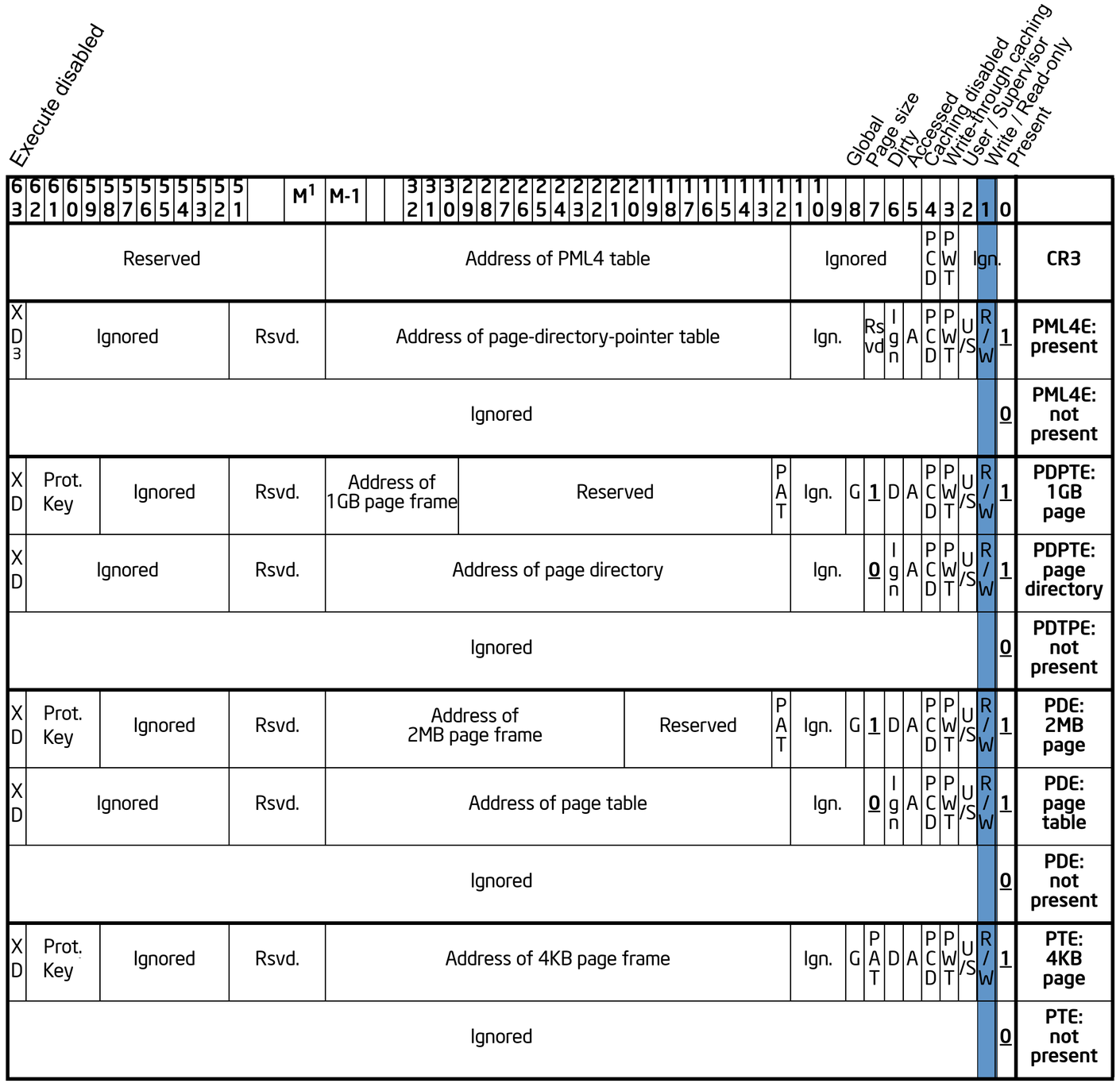

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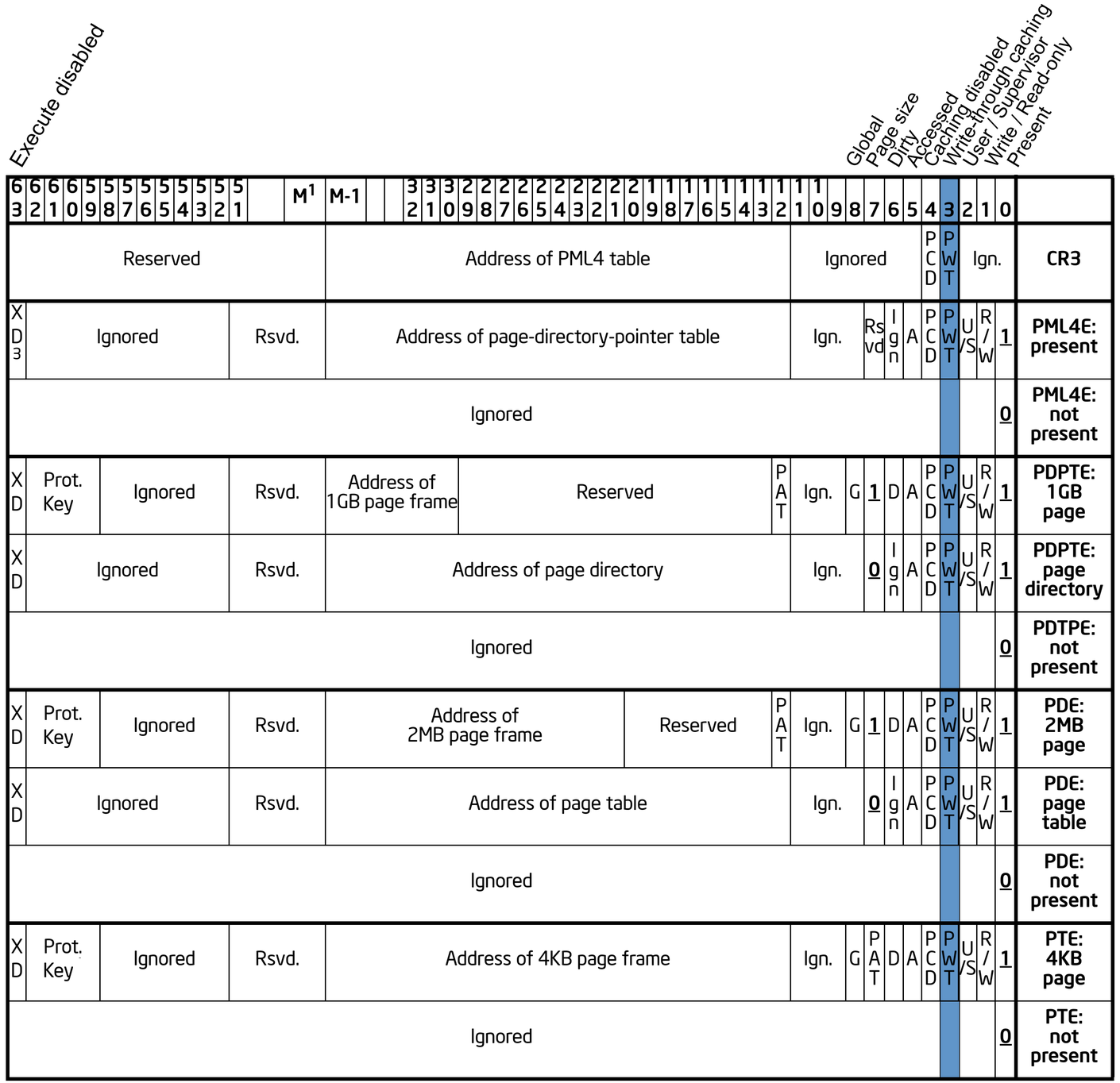

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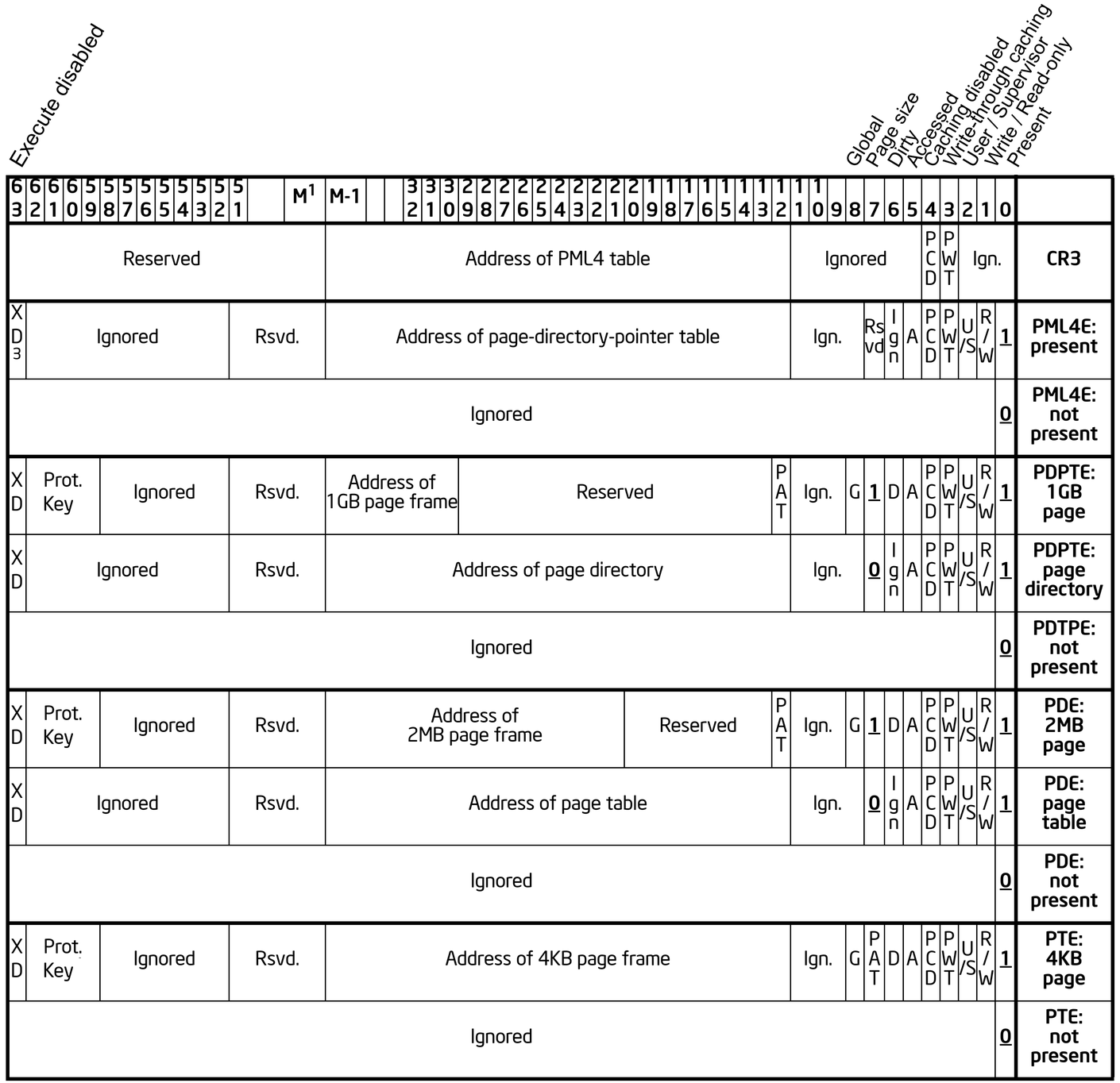

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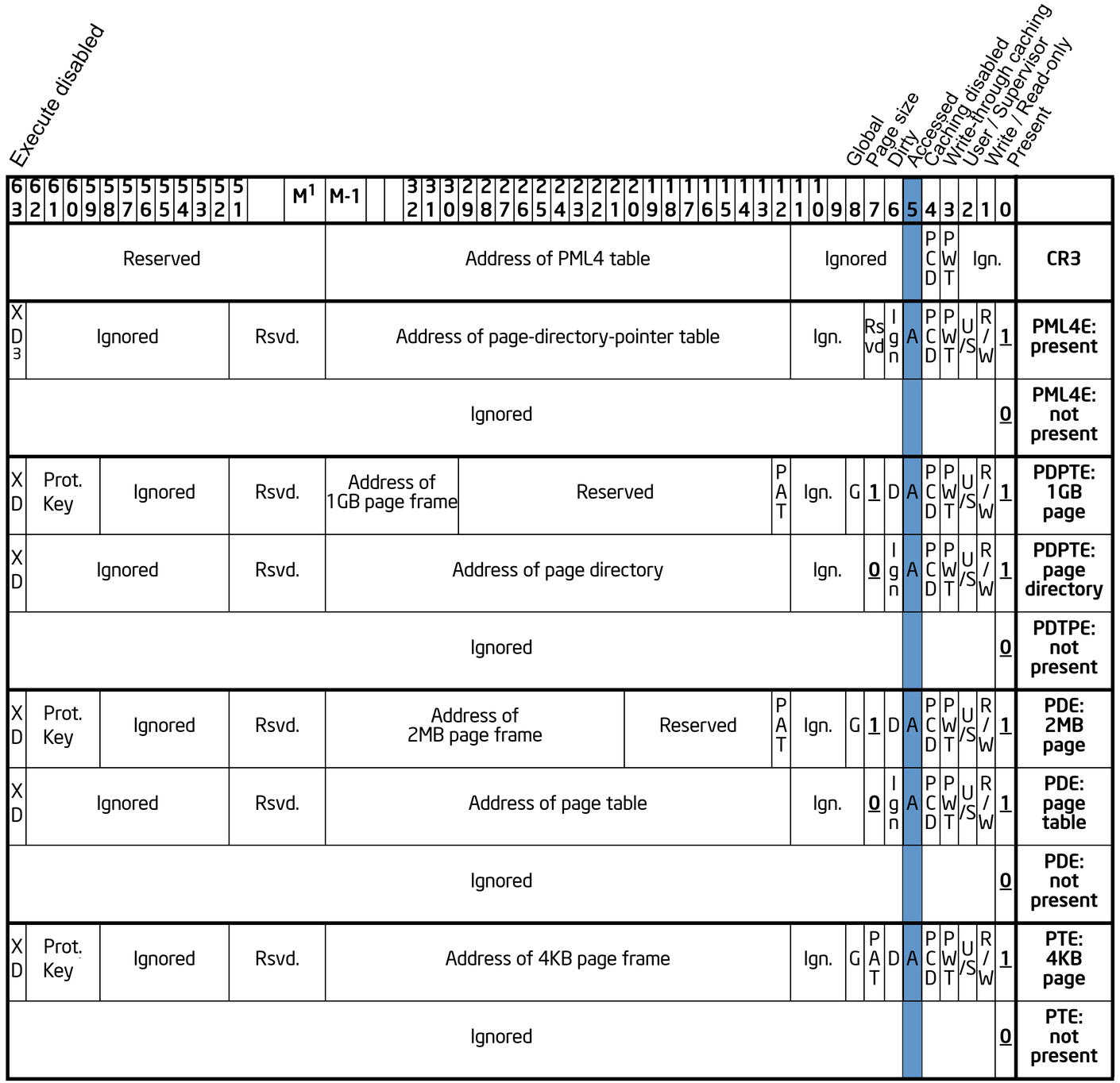

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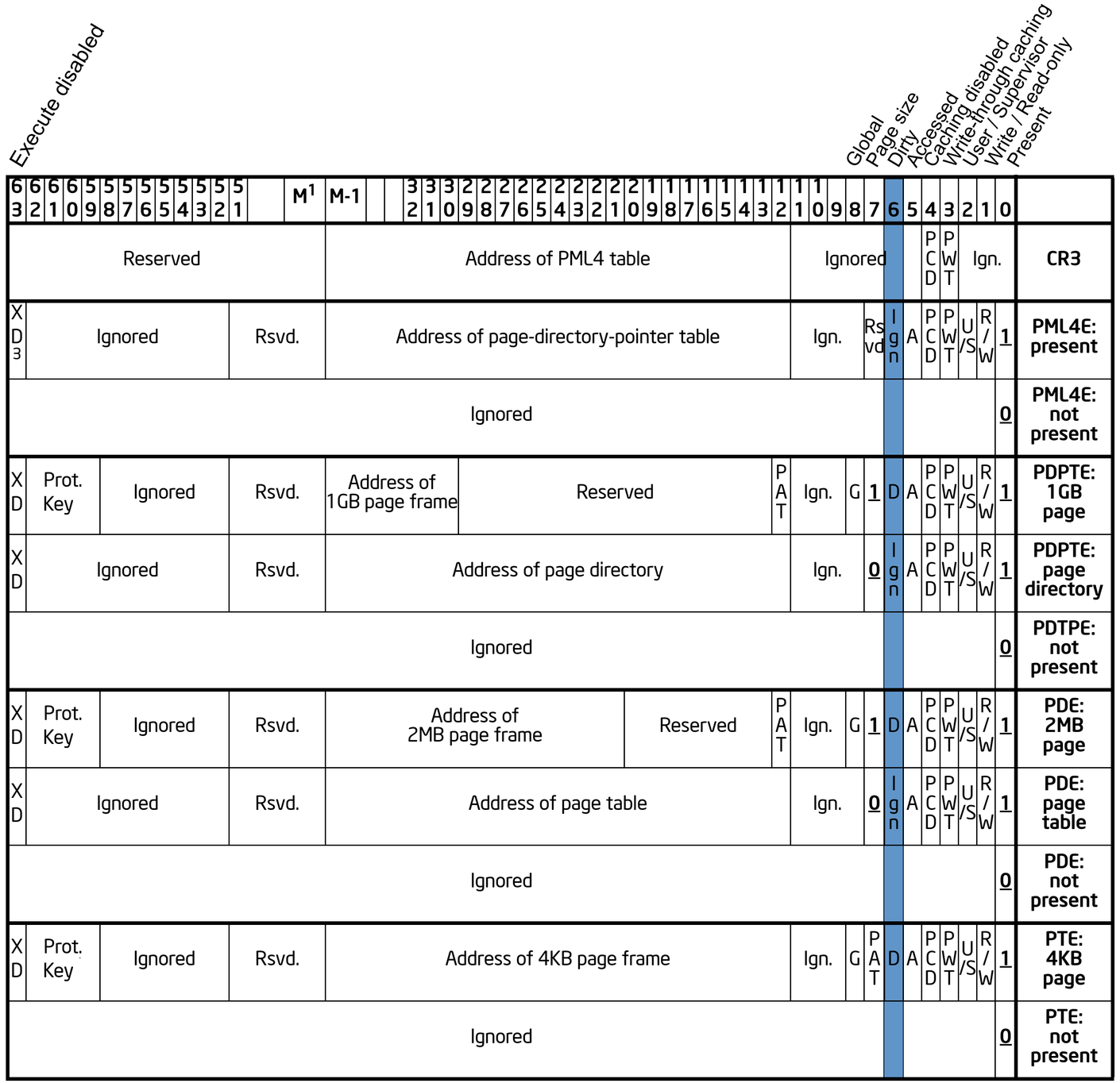

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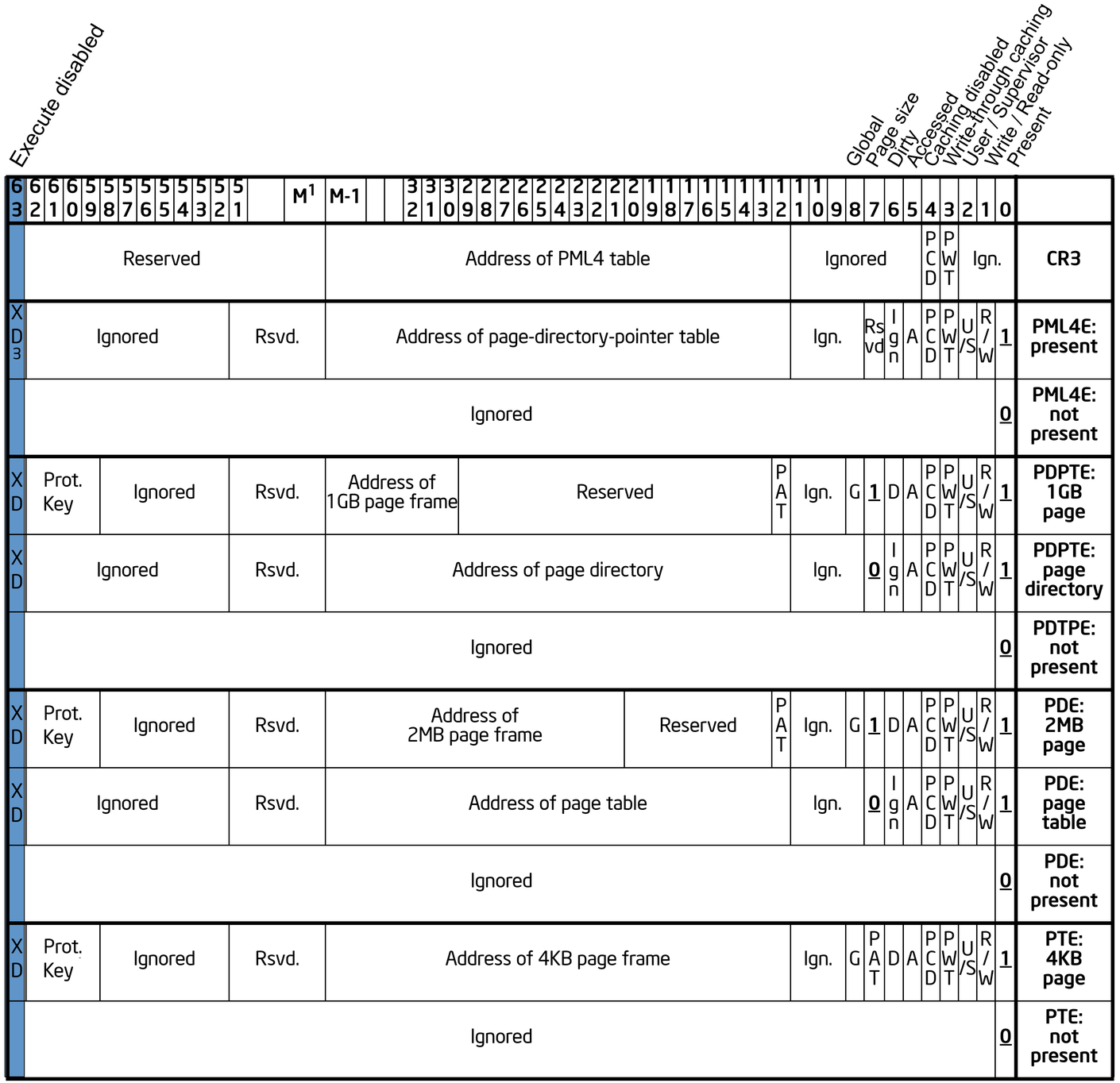

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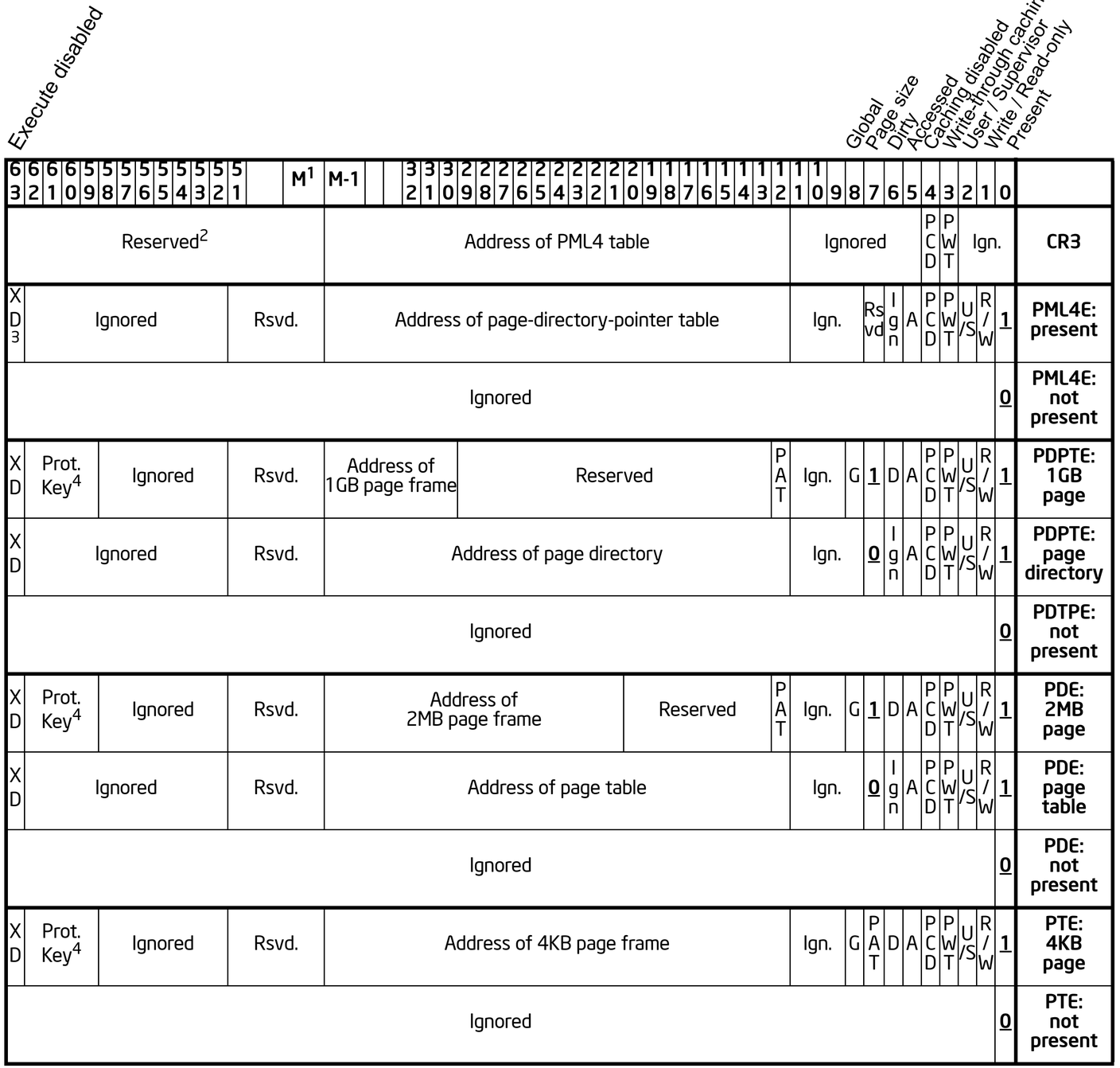

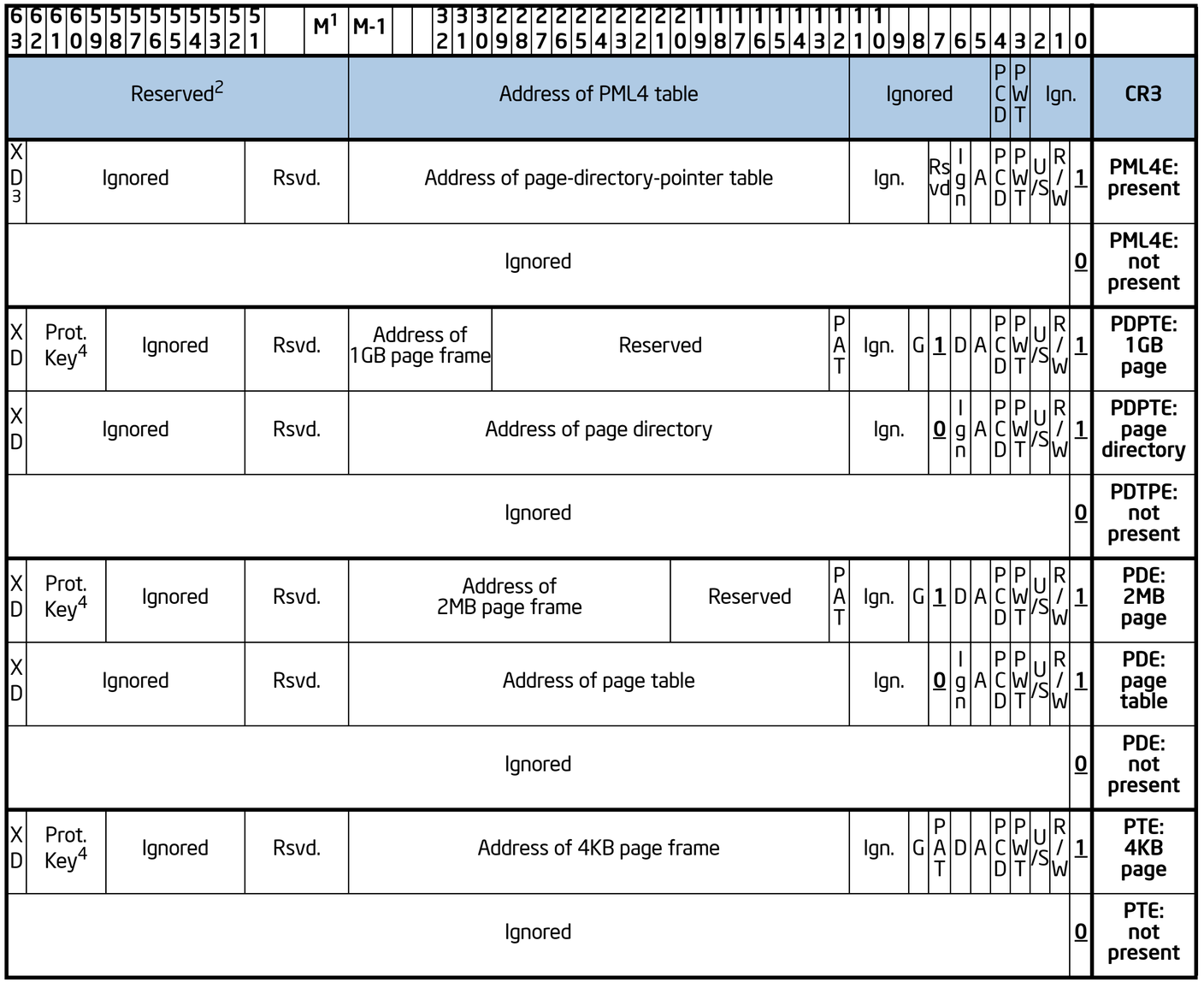

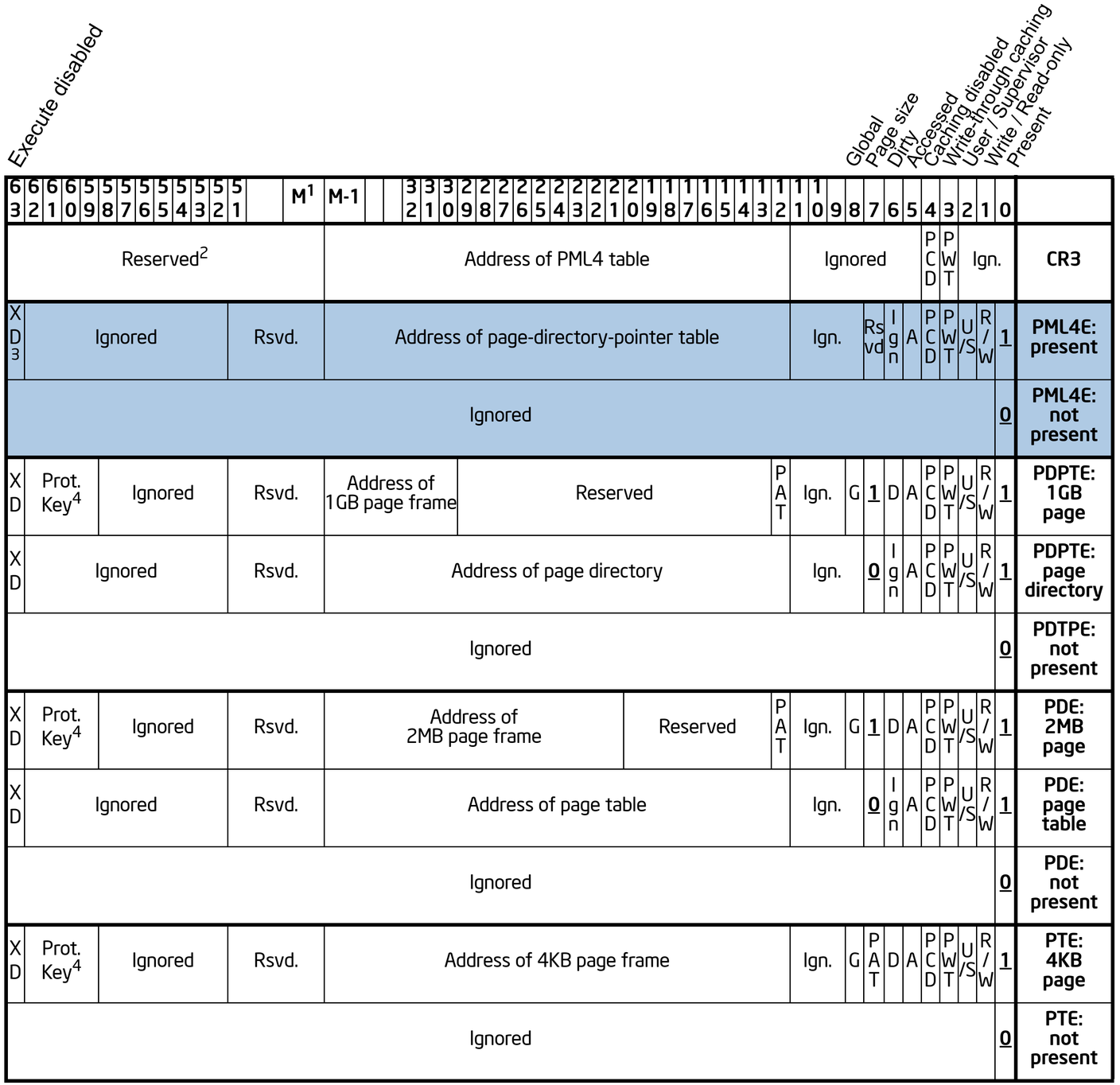

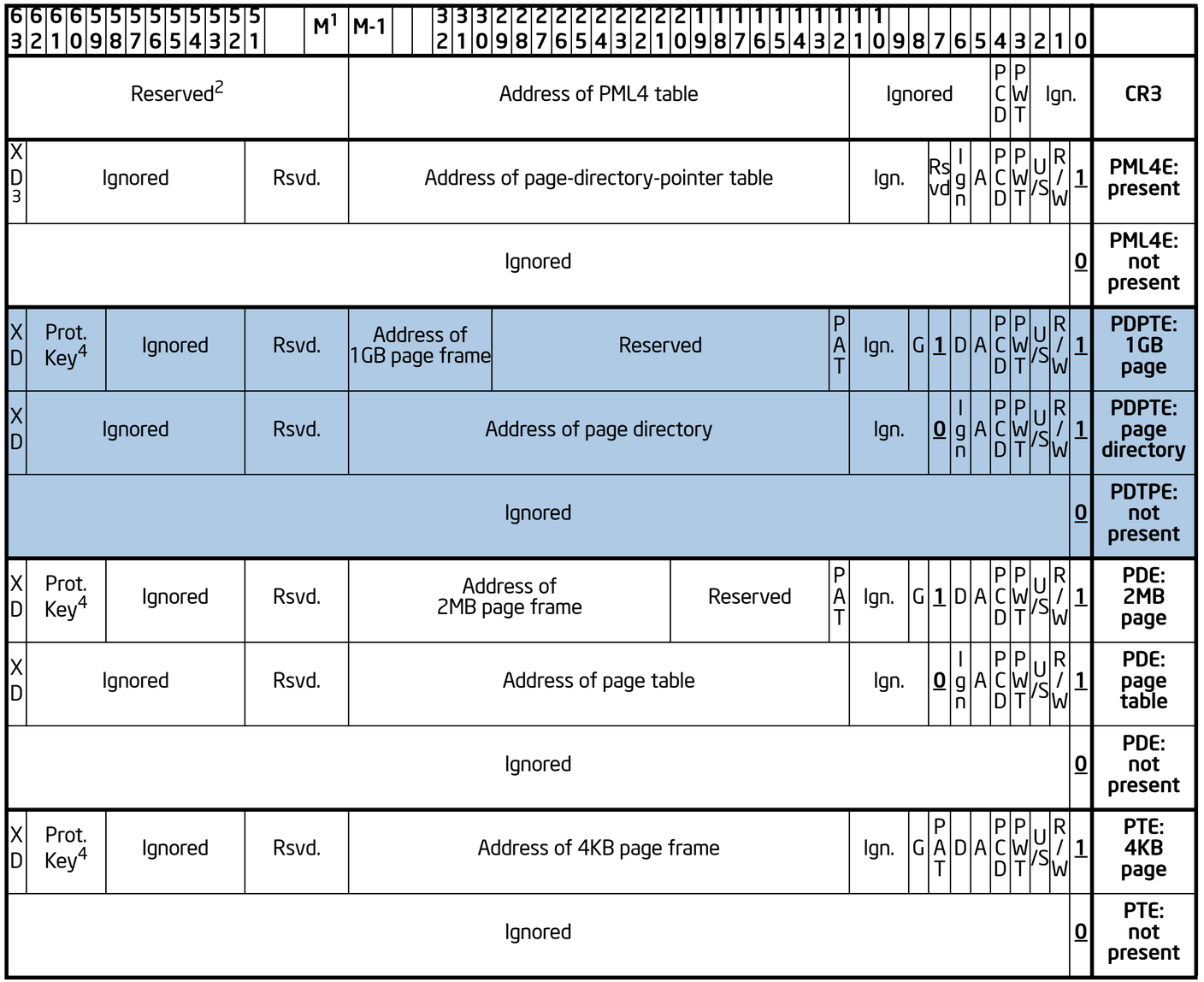

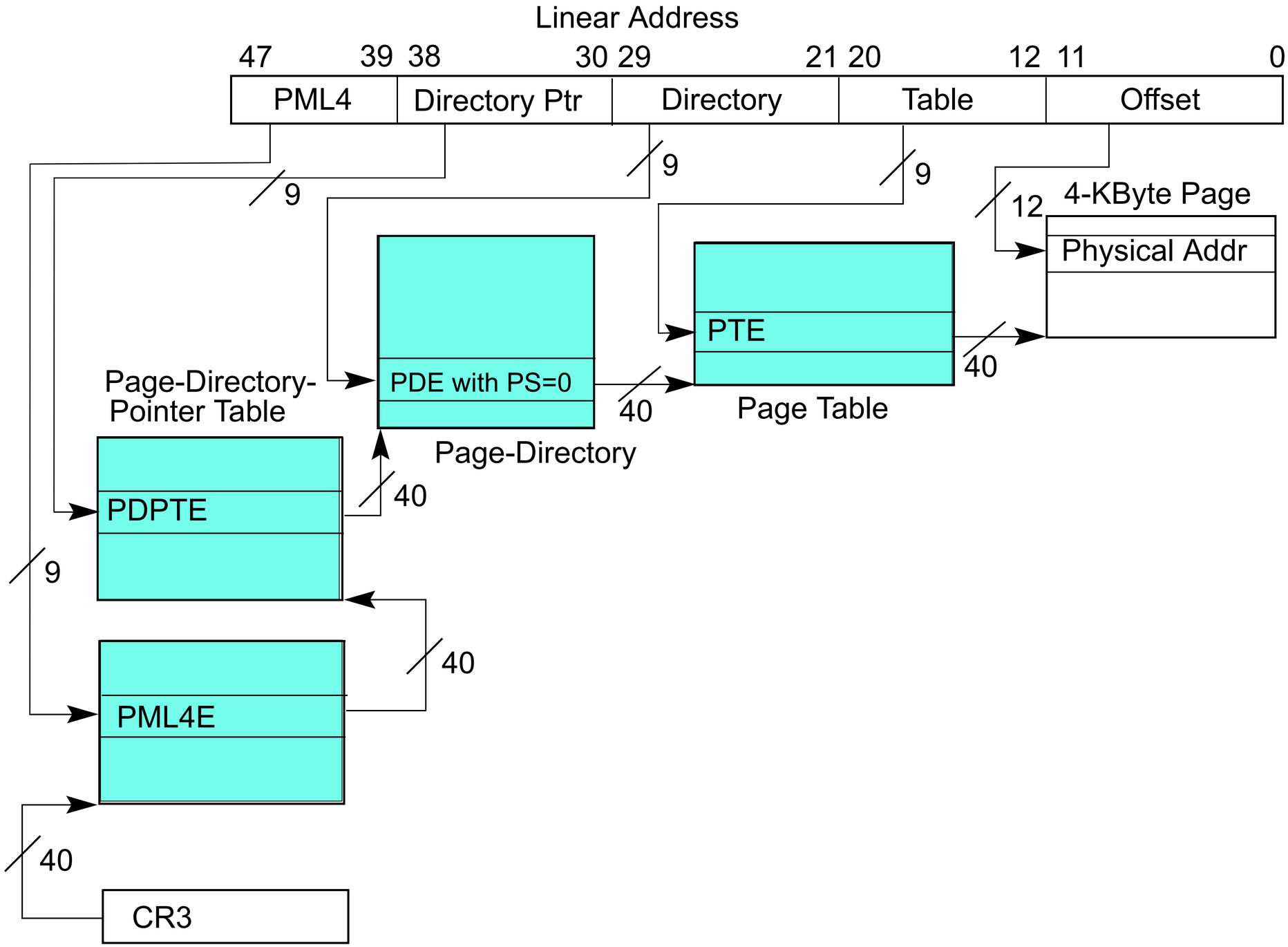
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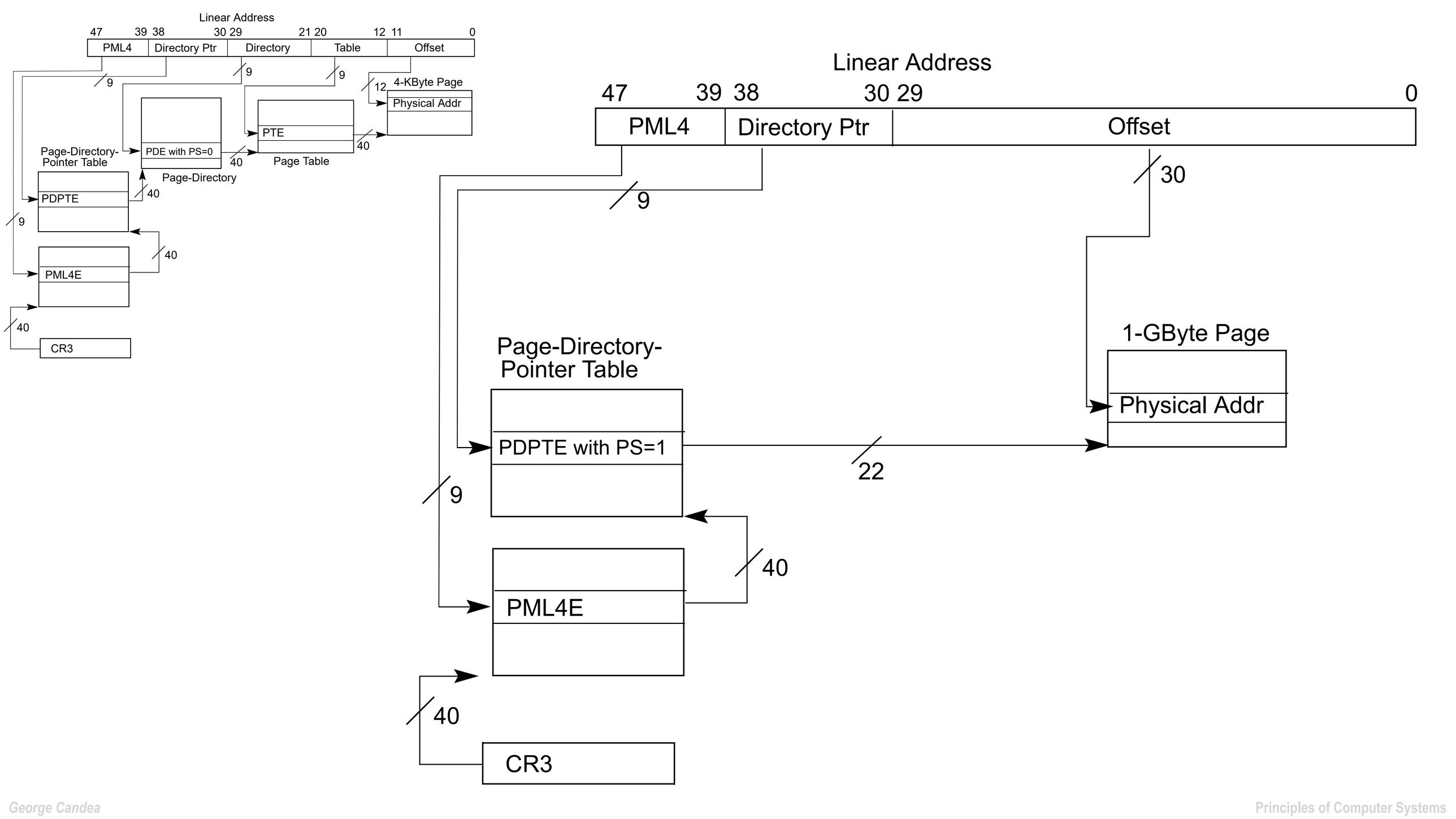
39
38
30
29
21
20
12
11
0
PML4
Directory Ptr
Directory
Table
Offset
9
9
9
12
4-KByte Page
Physical Addr
PTE
PDE with PS=0
Page-Directory-
Pointer Table
40
40
Page Table
Page-Directory
PDPTE
40
9
PML4E
40
40
CR3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PDPTE with PS=1
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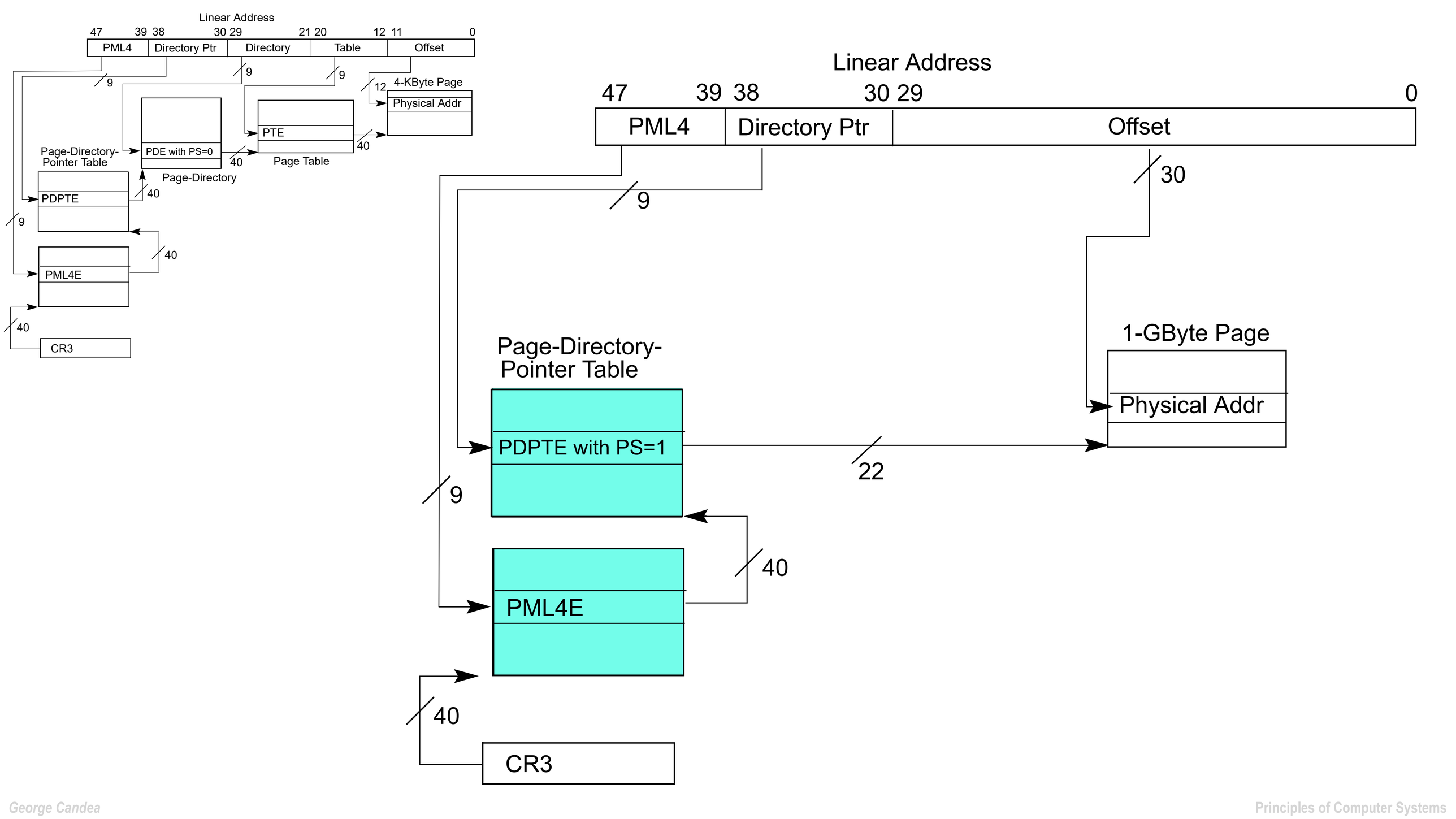
CR3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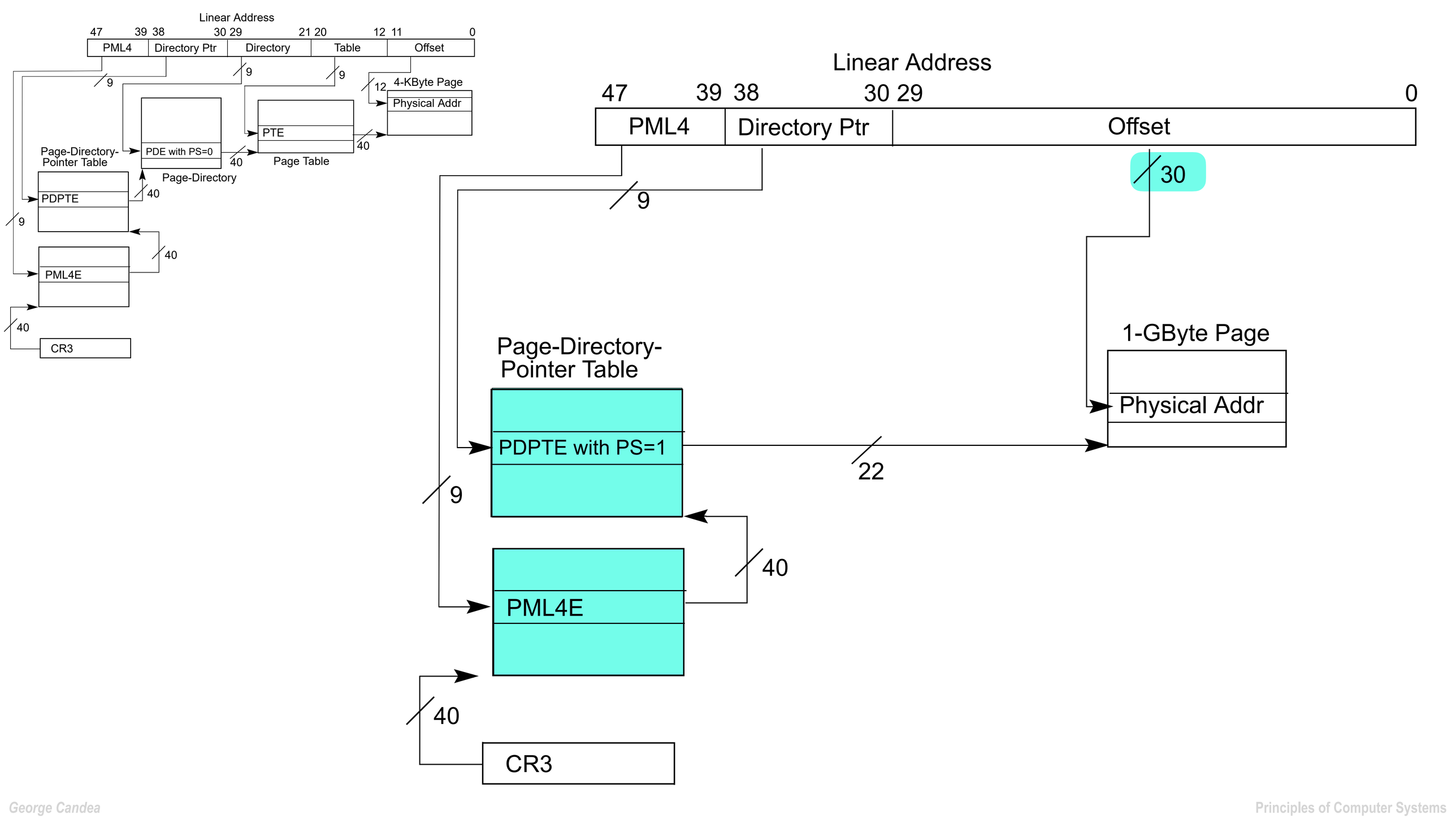
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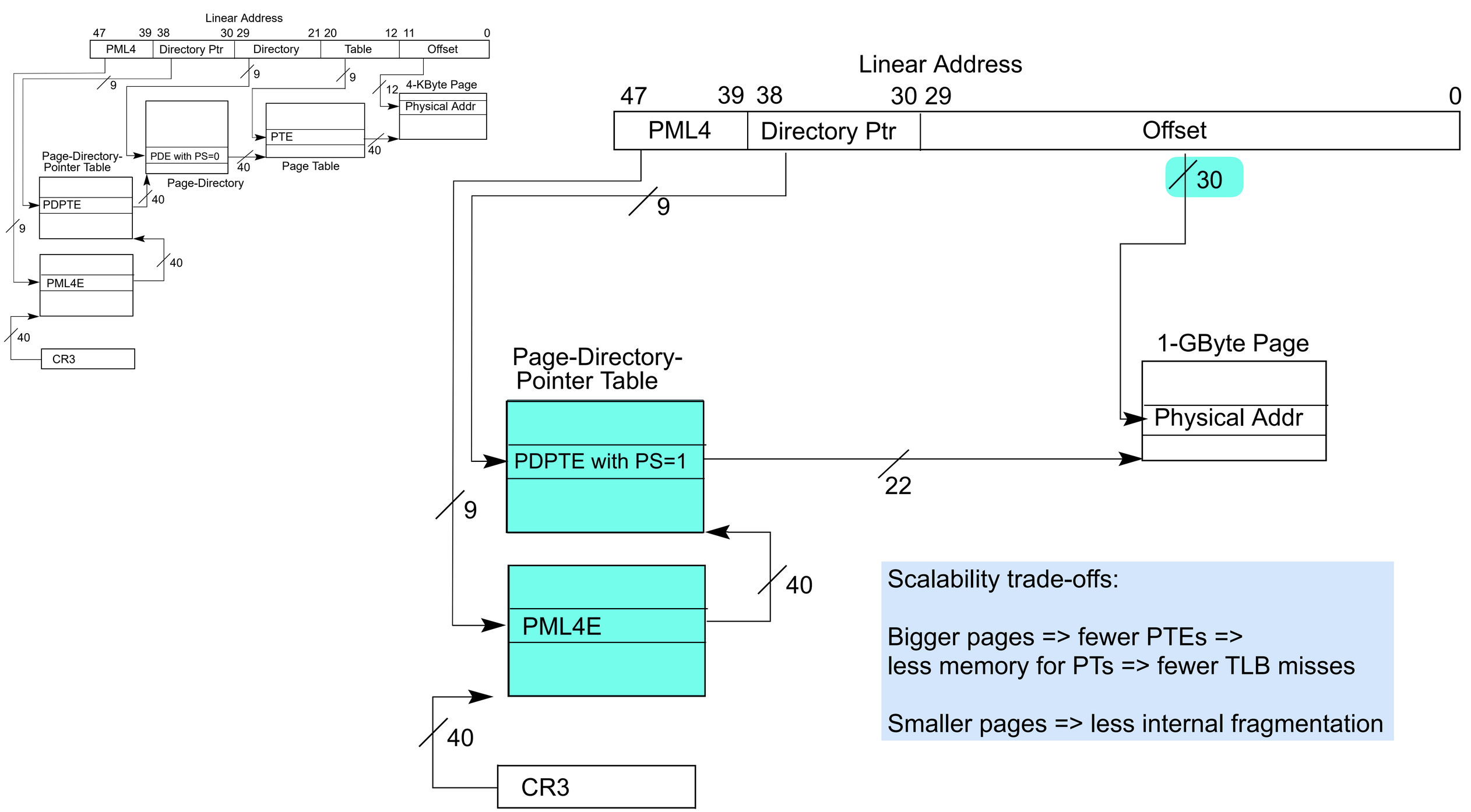
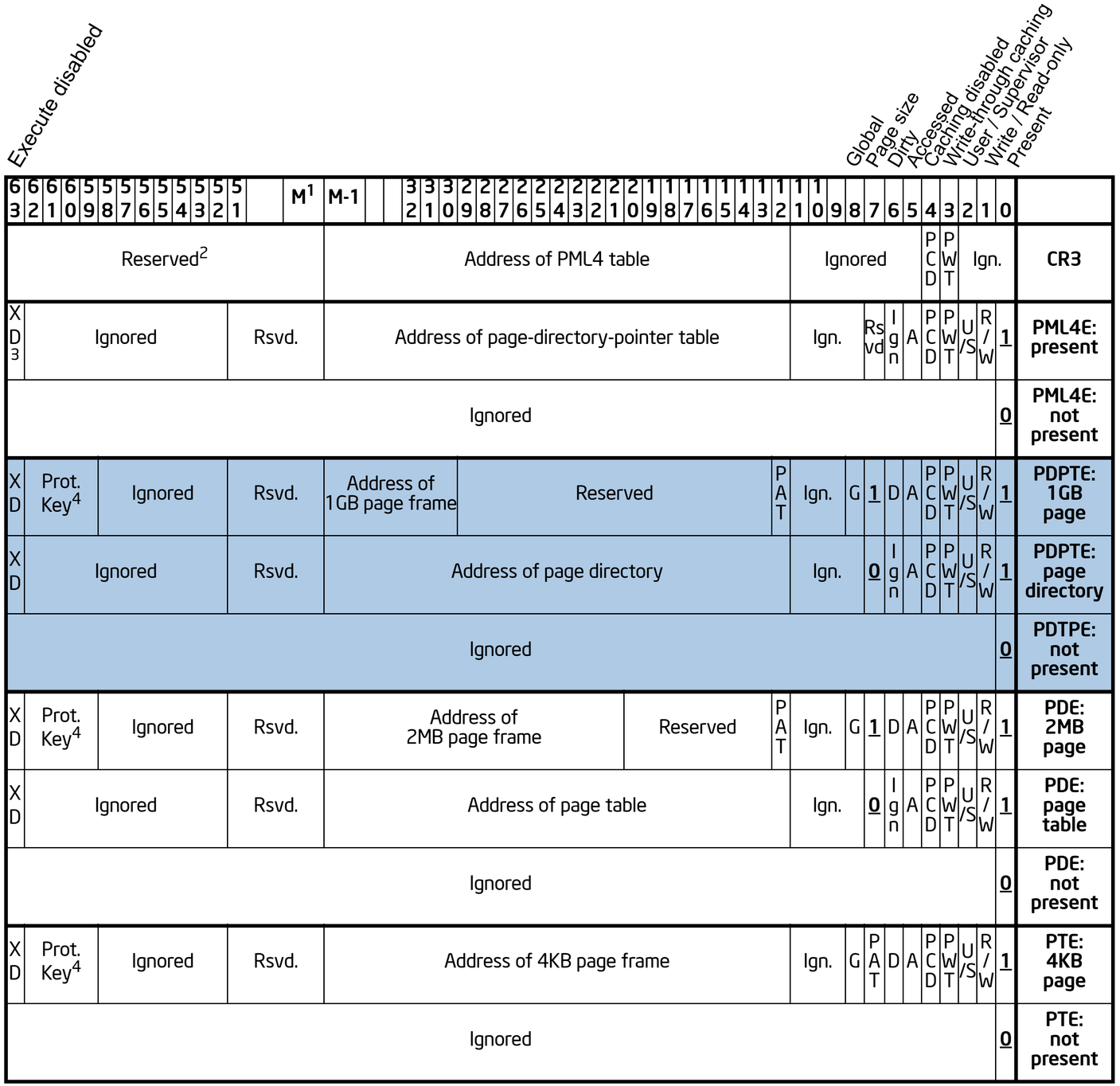
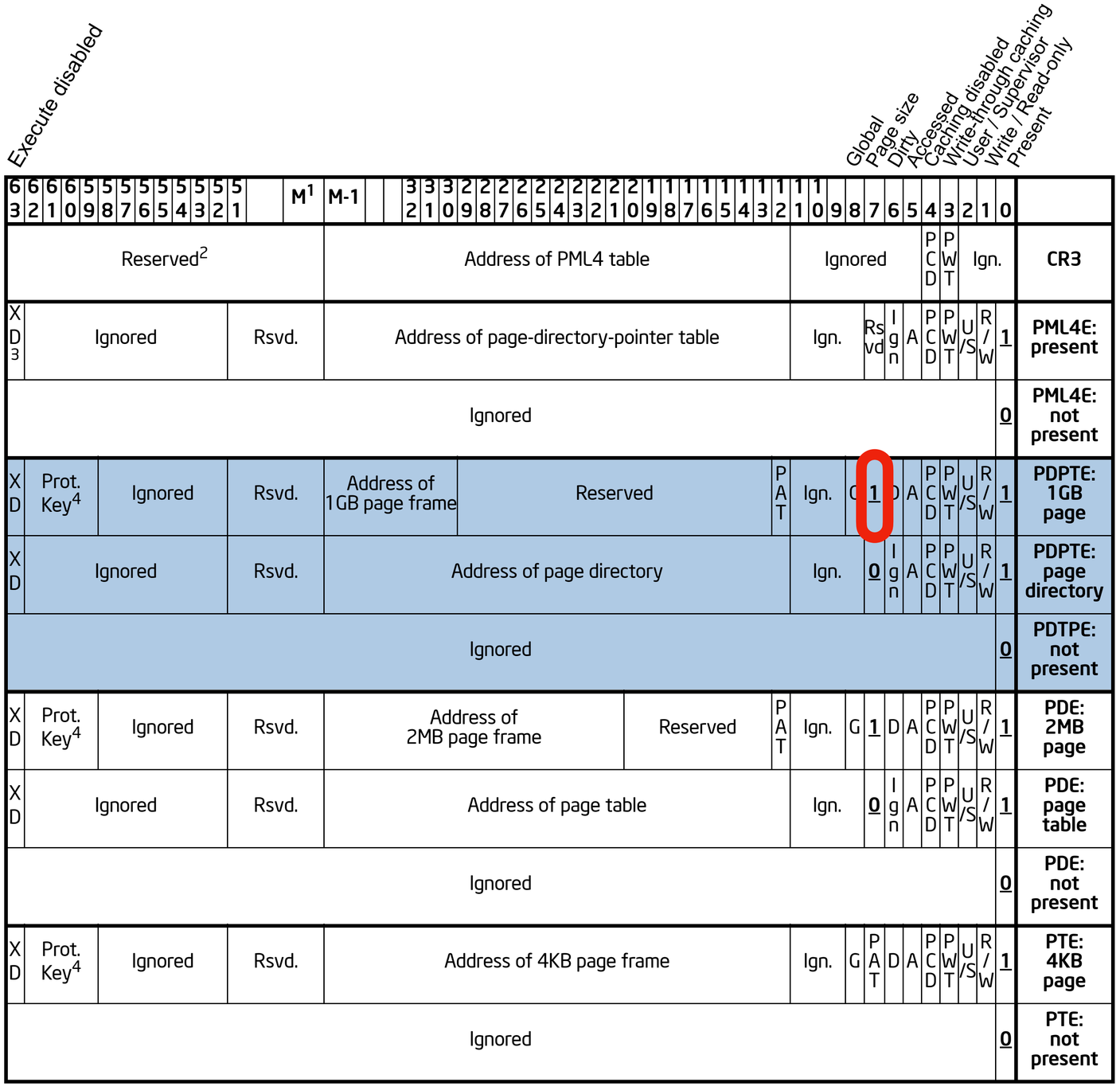


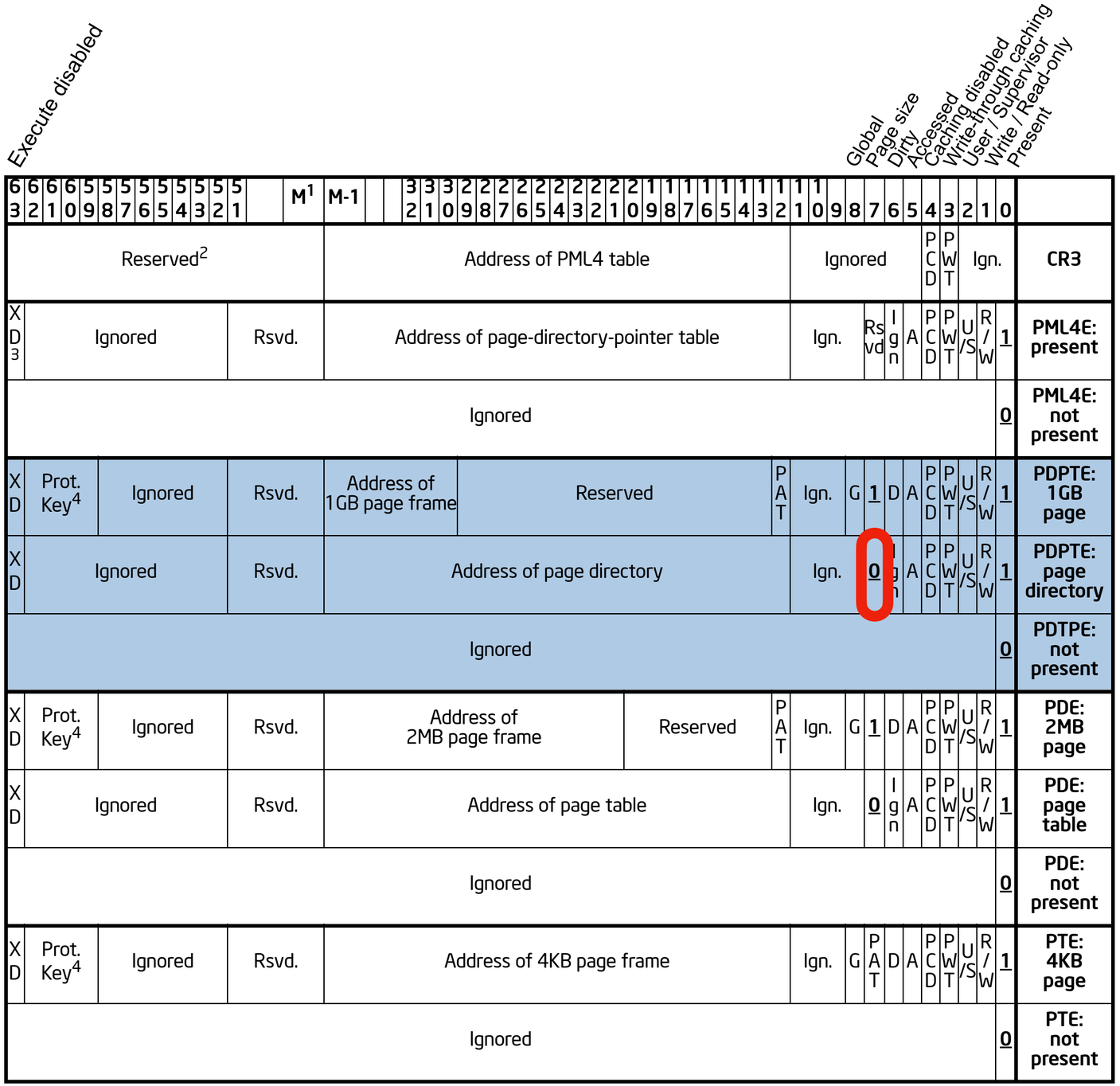
Scalability trade-offs:

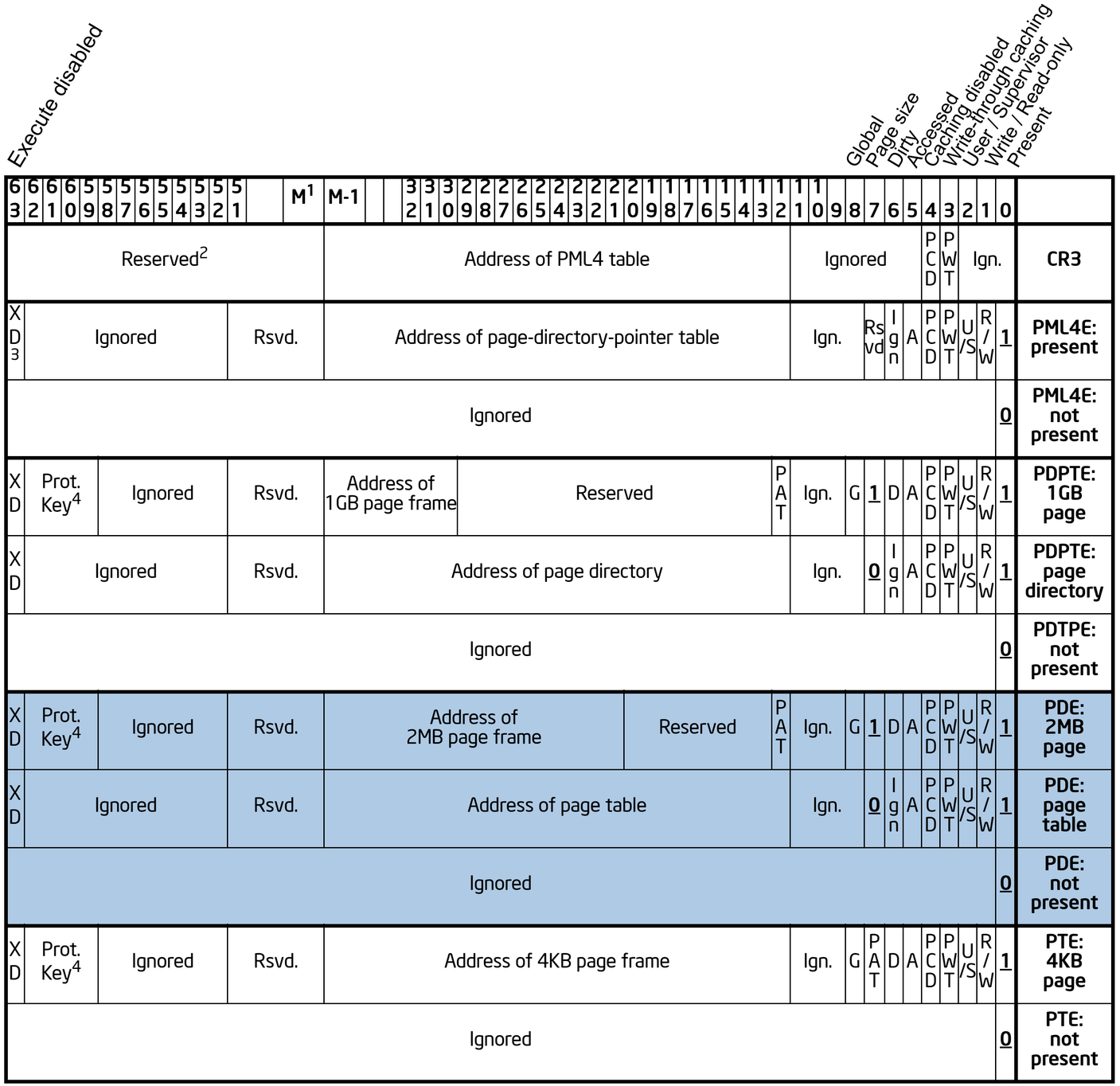
Bigger pages => fewer PTEs =>
less memory for PTs => fewer TLB misses

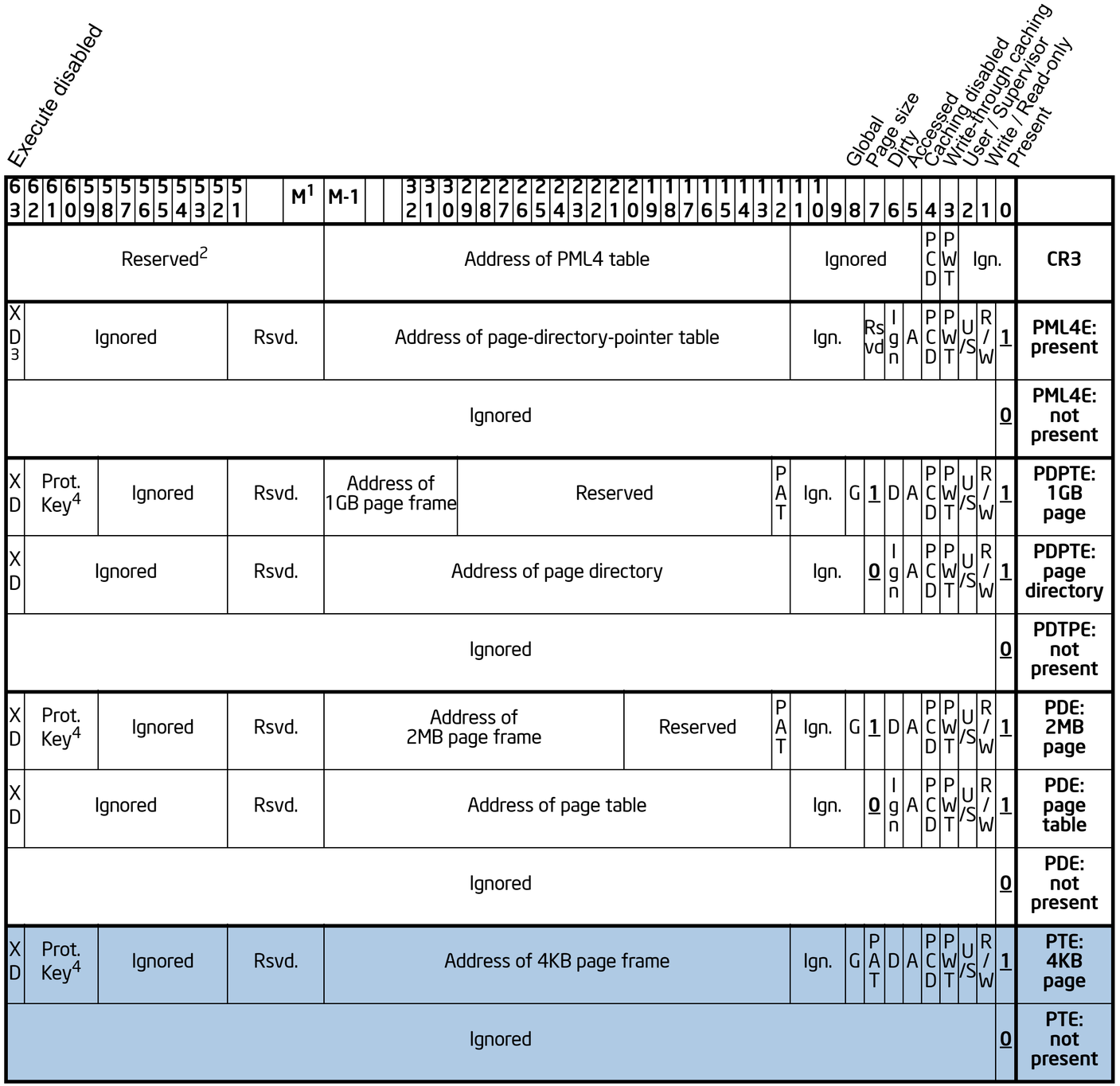
Smaller pages => less internal fragmentation

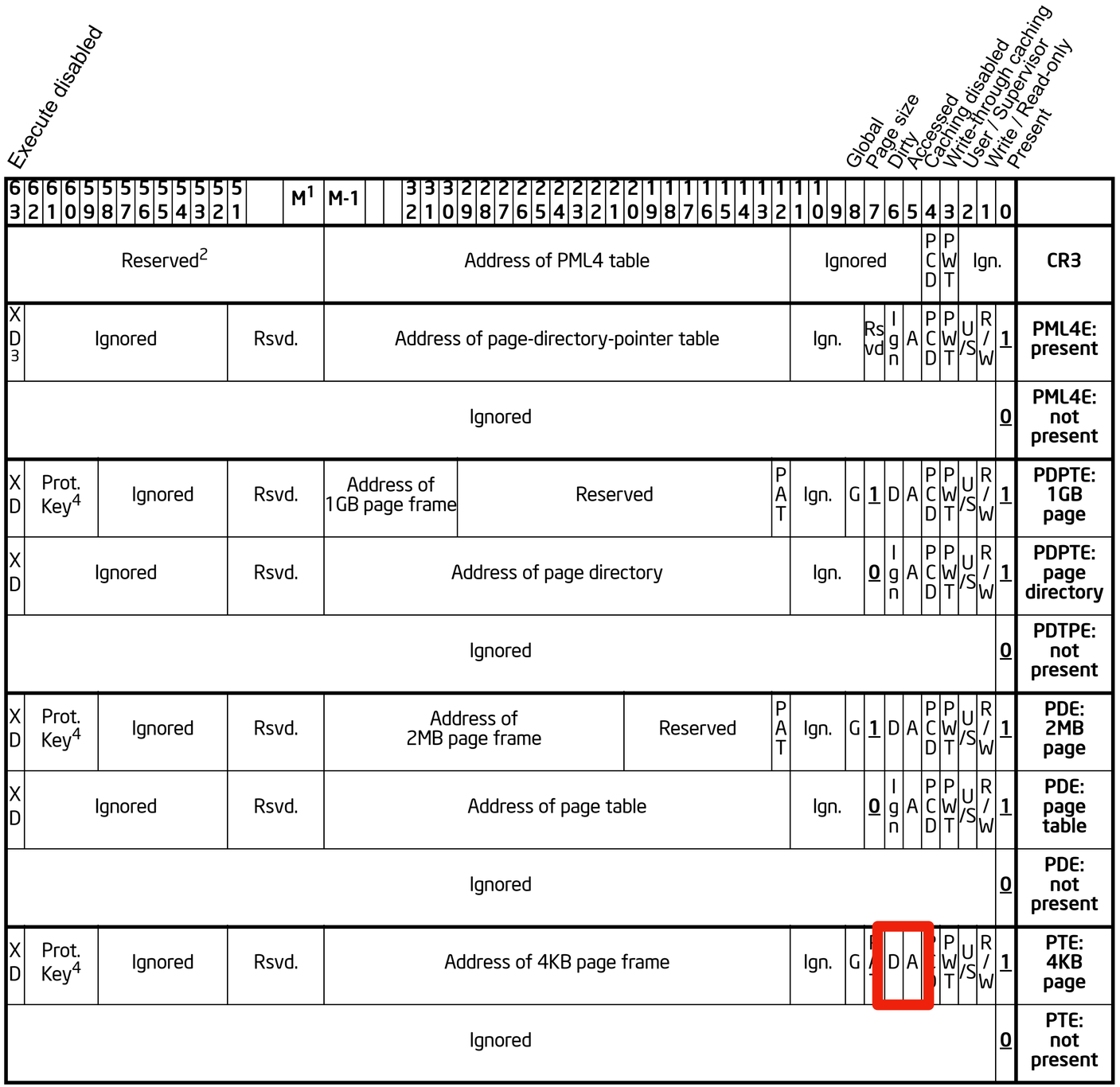


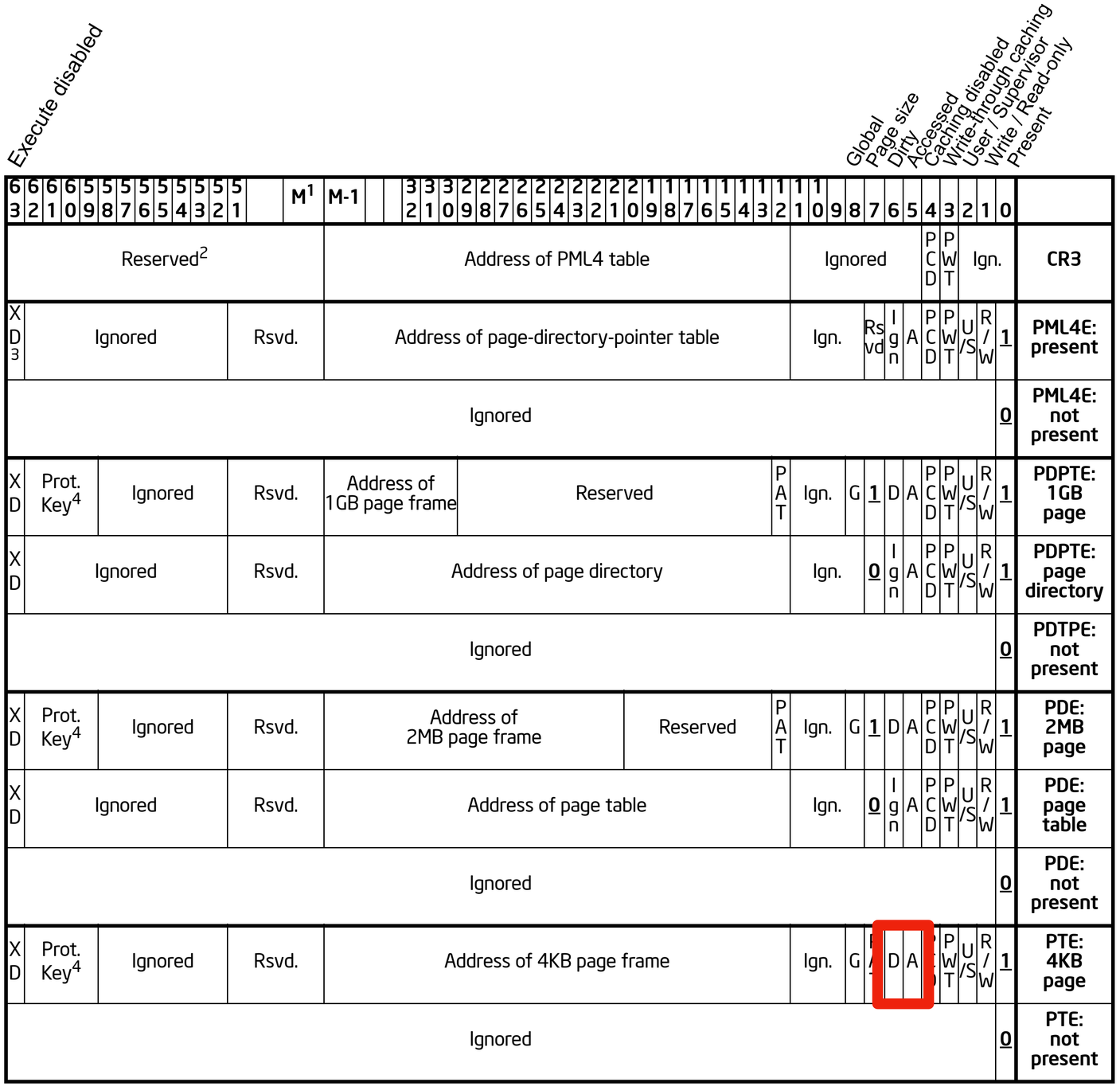












4 x 50 ns table lookup +
1 x 50 ns access =
250 ns =
~750 instructions @ 3 GHz clock

I could be doing a lot of useful work while waiting to read memory !

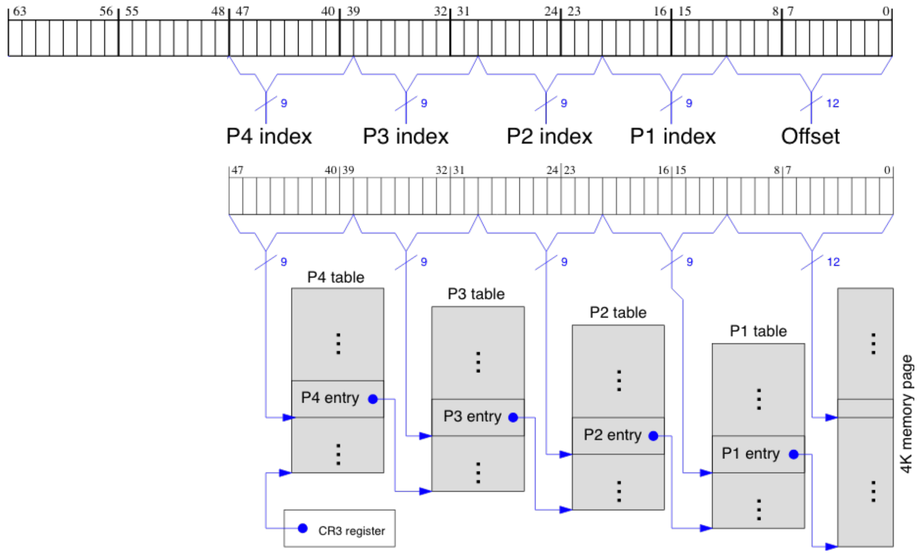
What to do ?

Intel® 64 and IA-32 Architectures Software Developer's Manual . Volume 3: System Programming Guide, May 2018

Caching Generalities

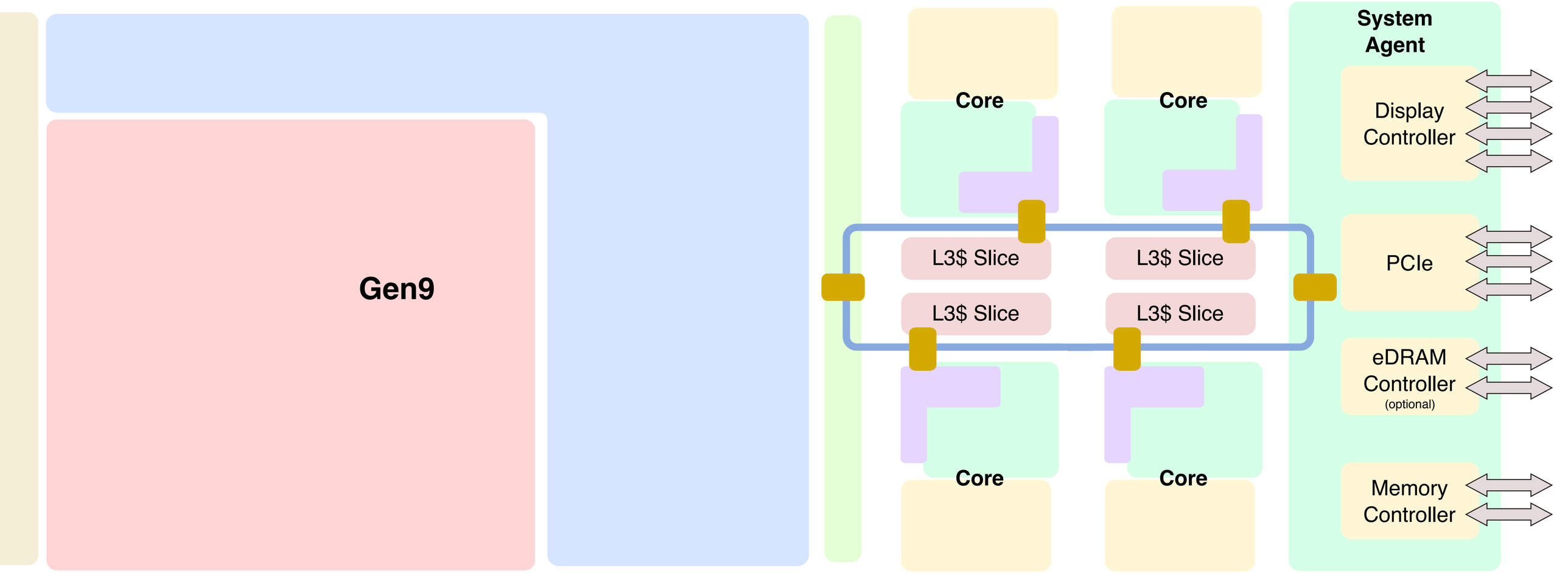
Recap of Key Concepts in Caching

- Locality
  - *temporal (reuse within short amount of time)*
  - *spatial (use shortly physically nearby data)*
- Replacement algorithm
  - *LRU, Time-aware LRU in CDNs, Least-frequent LRU in CDNs, MRU in scanning big data*
- Write-through vs. write-back
- Working set
- Direct-mapped vs. partially associative vs. fully associative
- Speed vs. size (and thus cost) trade-off



Caching & TLBs

Intel Skylake Microarchitecture



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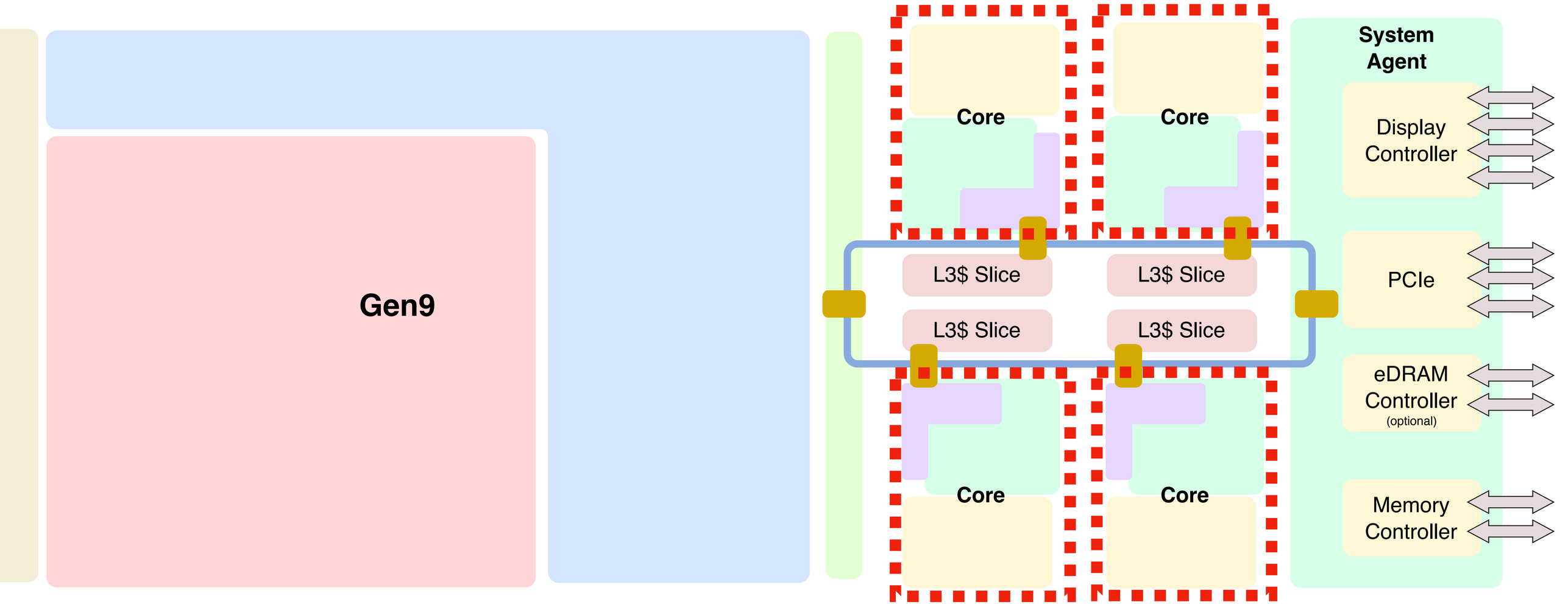

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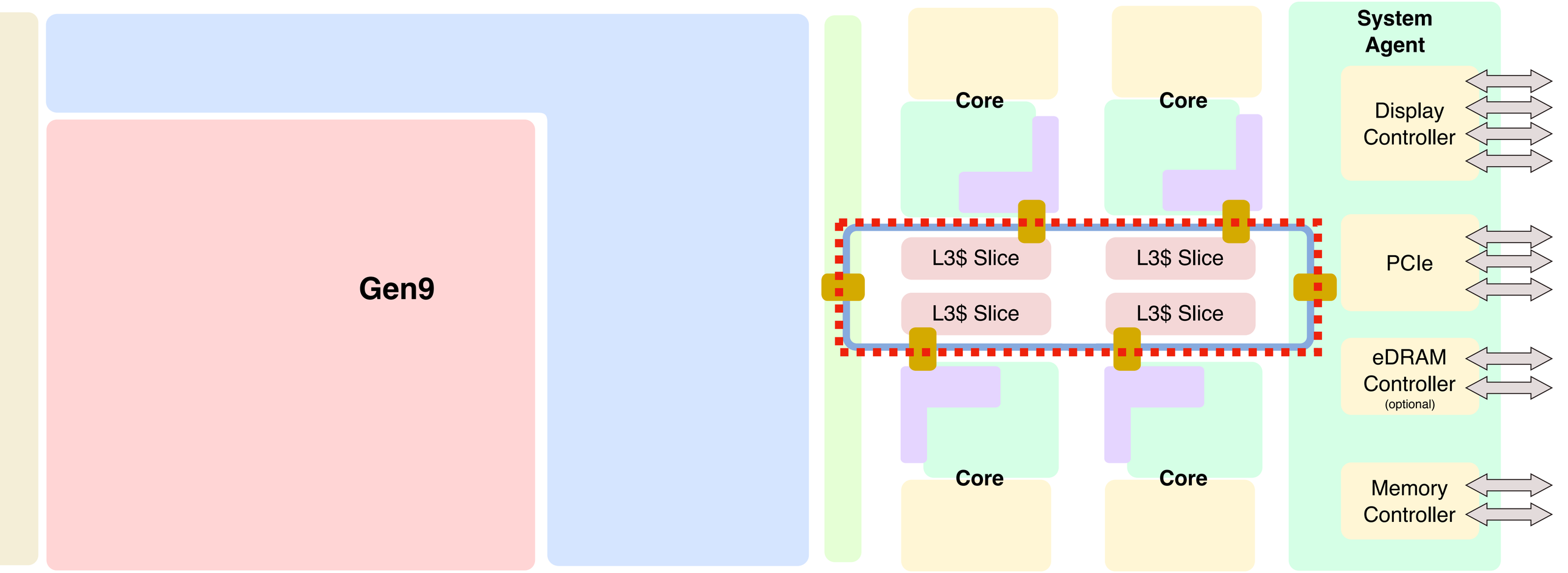

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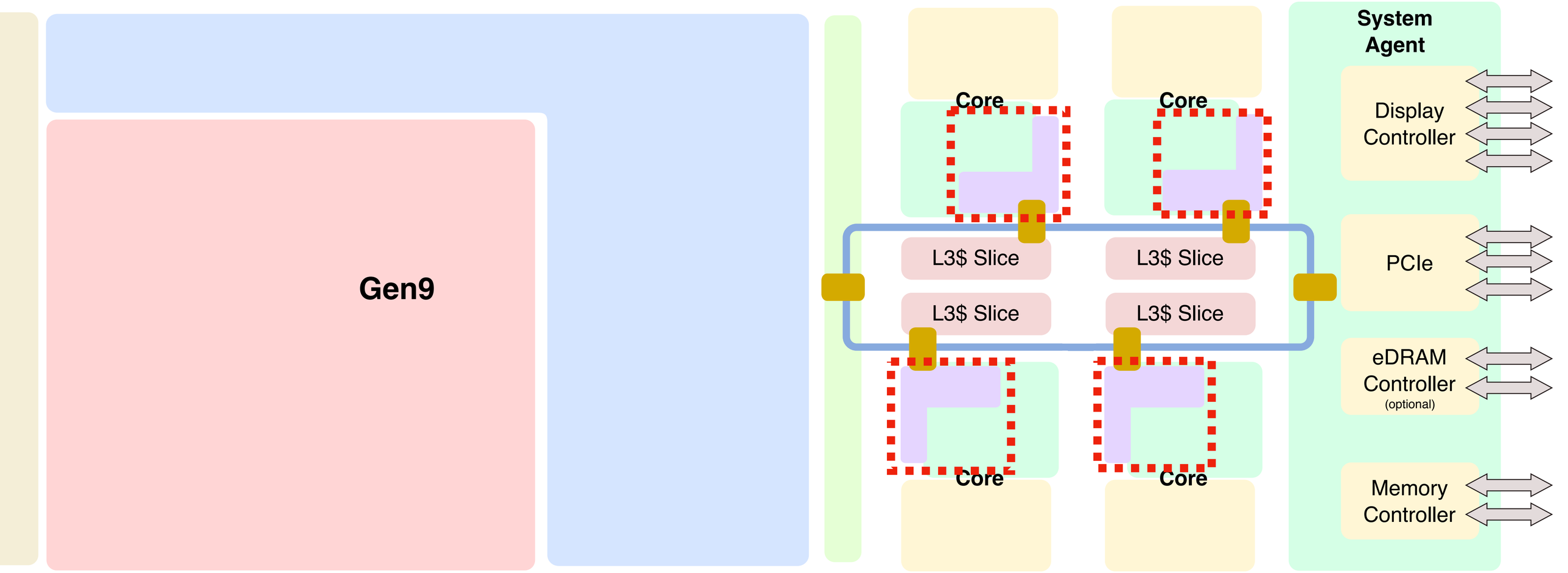

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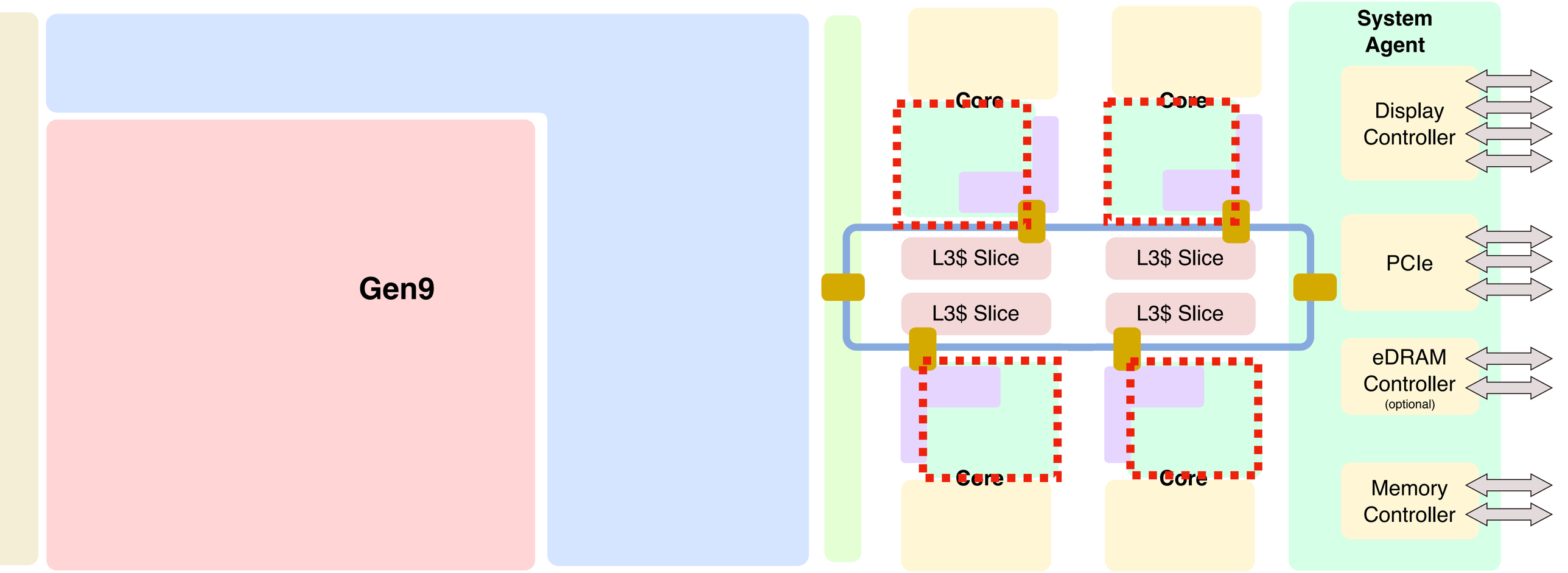

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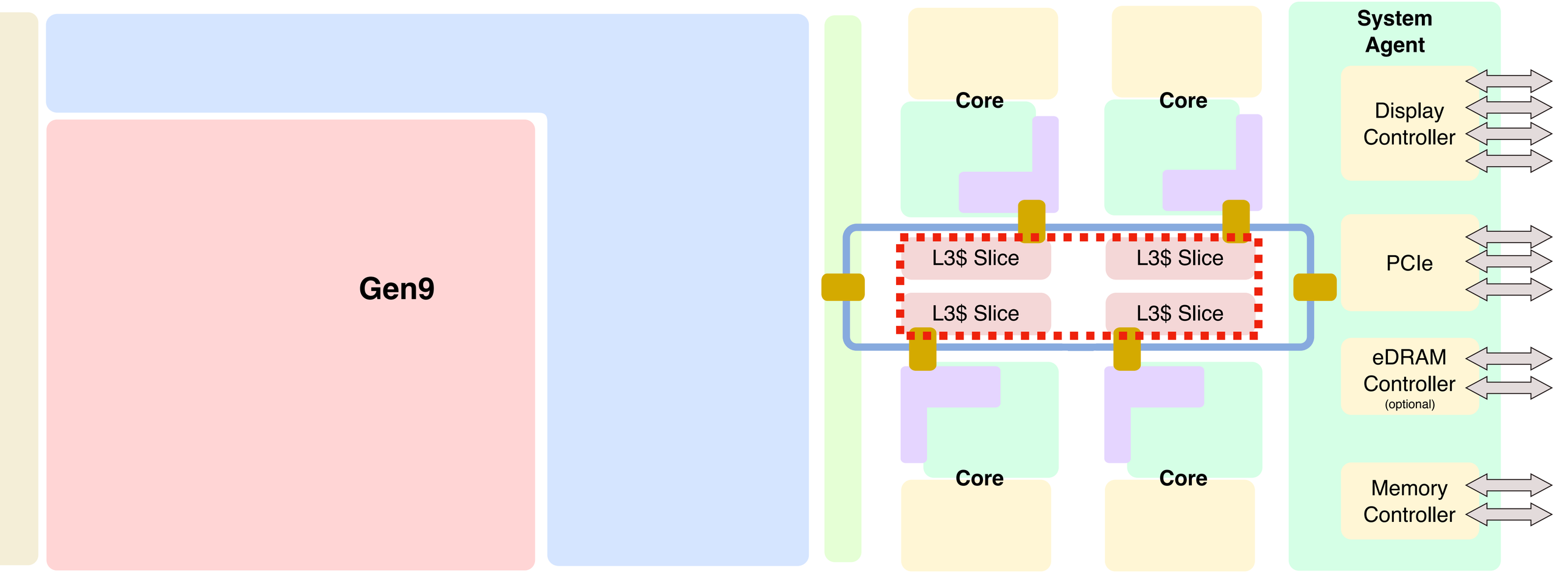

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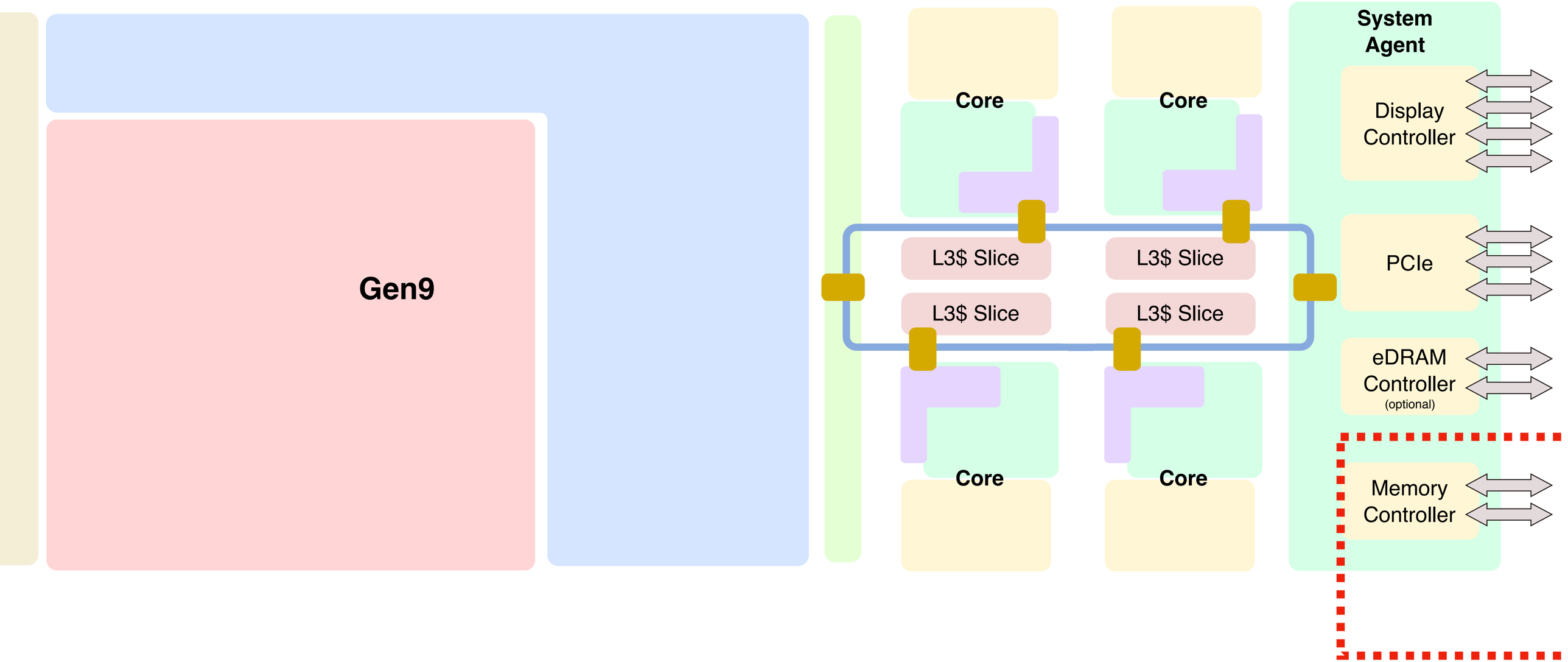
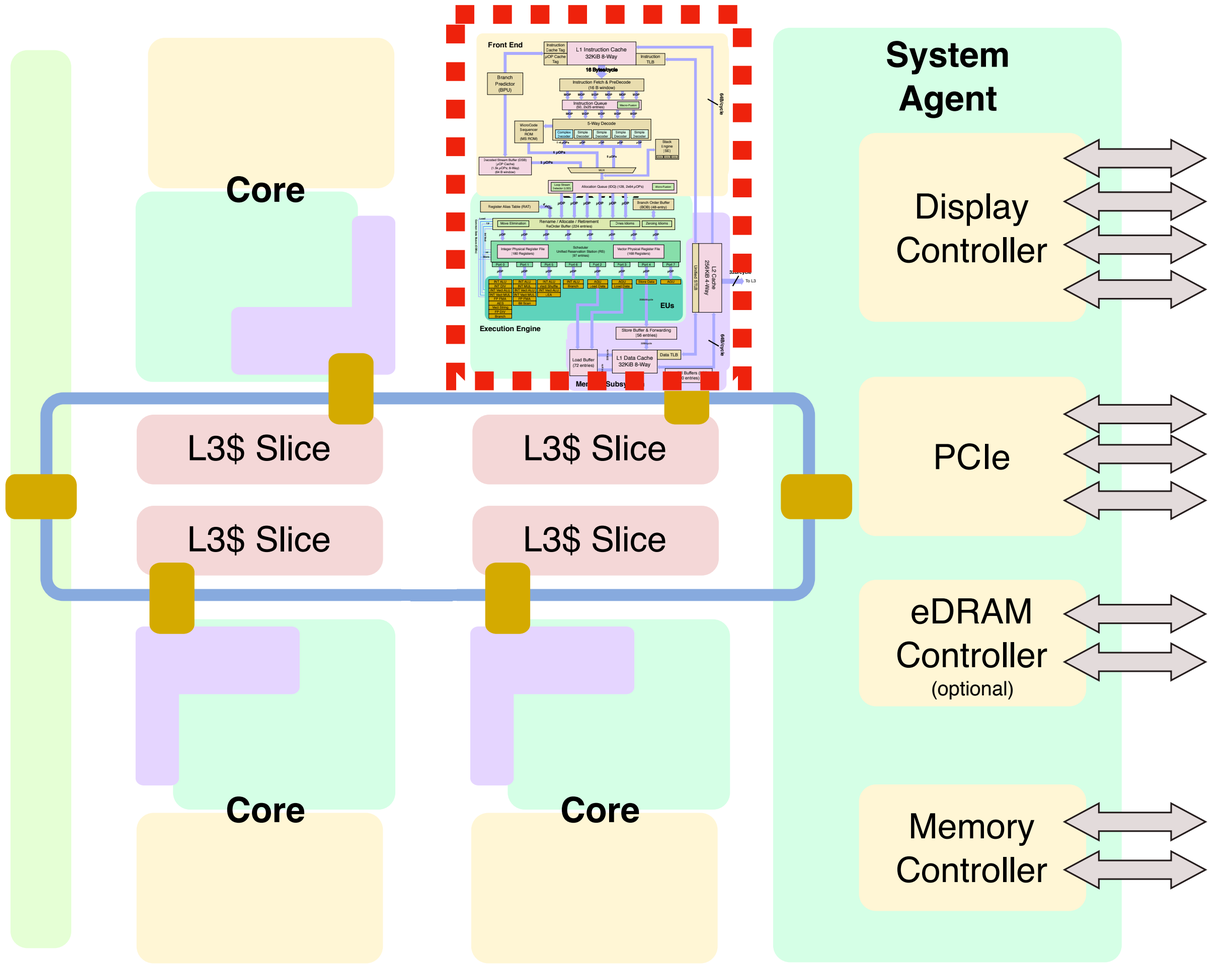
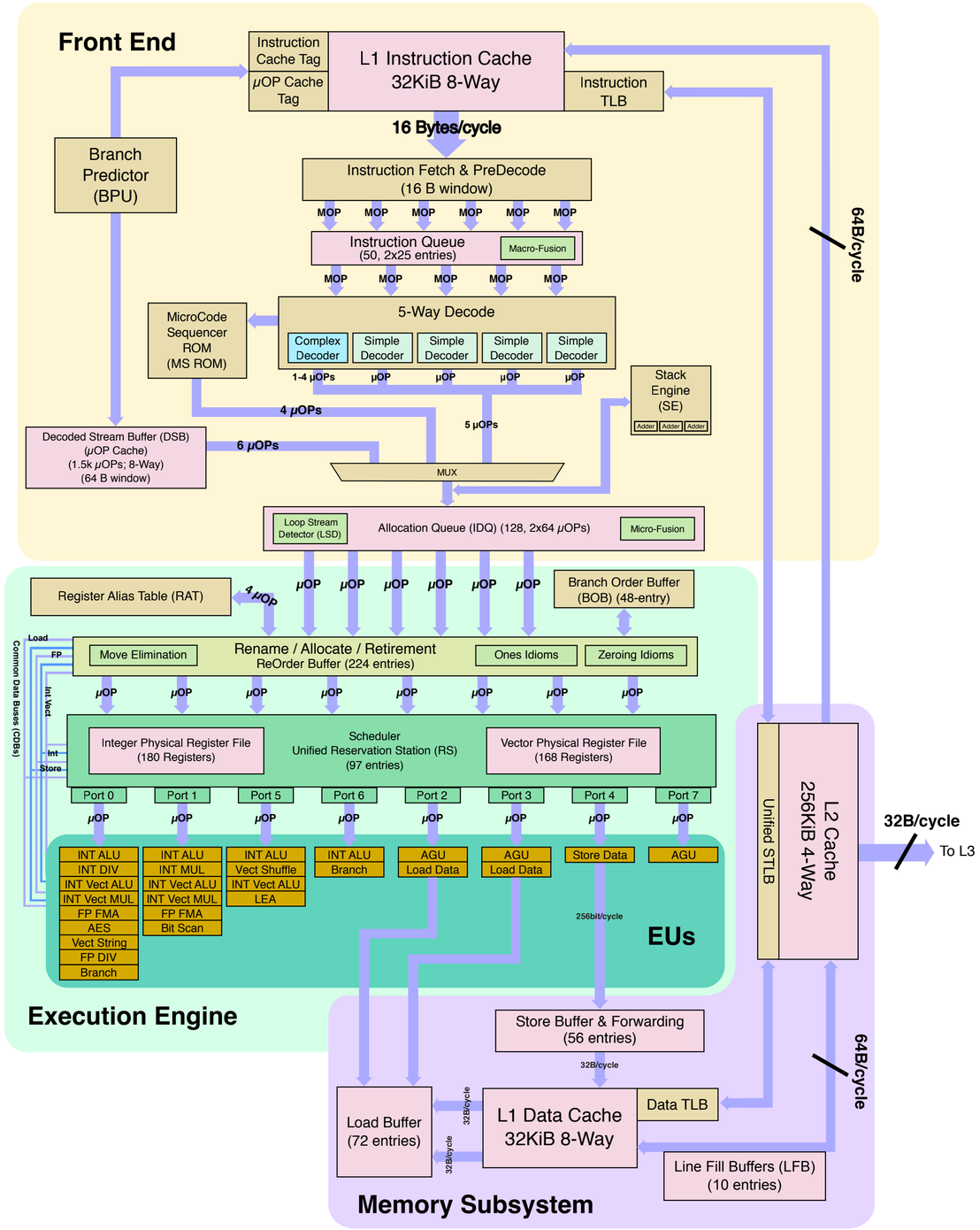
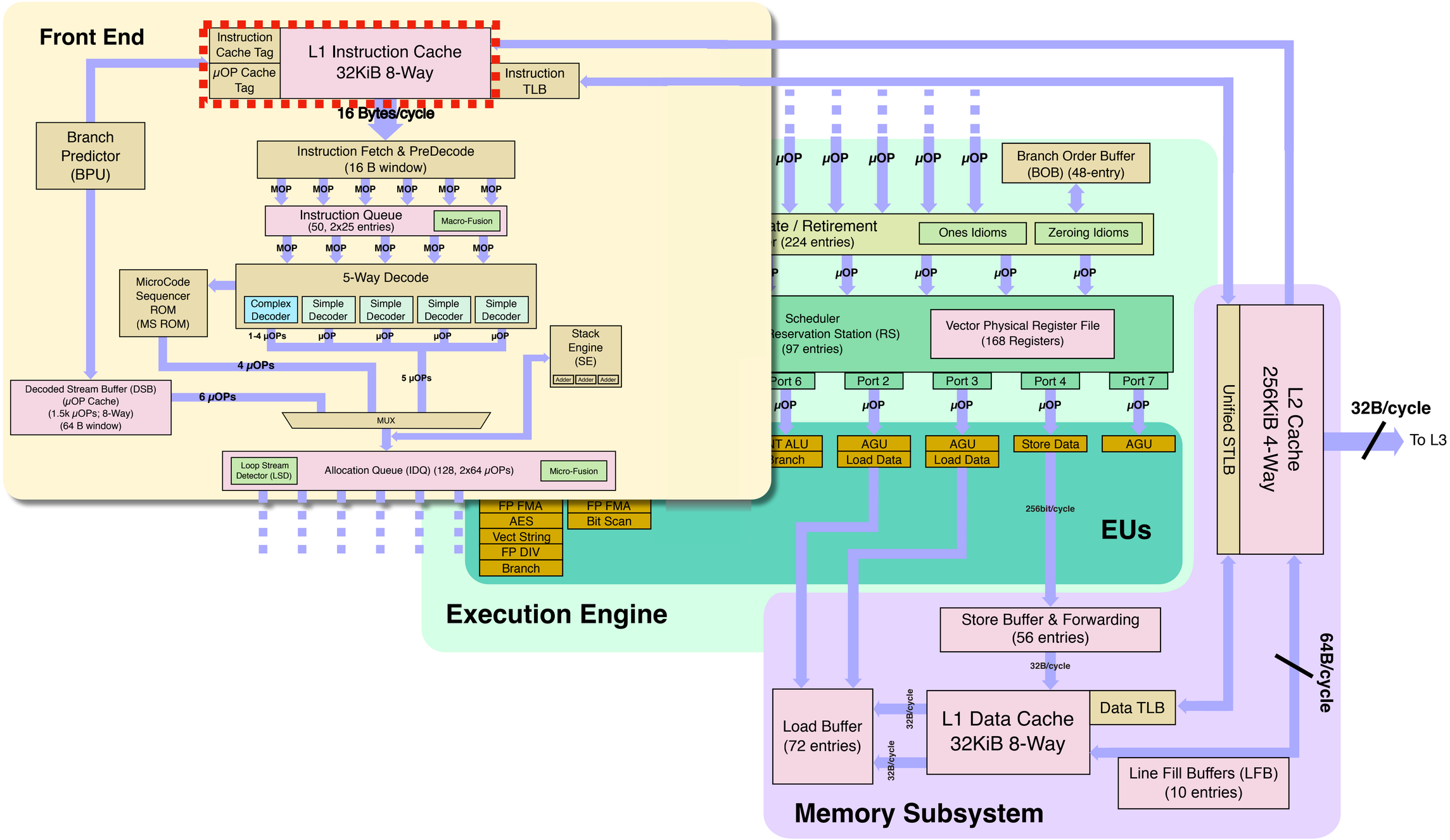


Intel Skylake Microarchitecture

Gen9




Front End
Instruction Cache Tag
µOP Cache Tag
L1 Instruction Cache 32KiB 8-Way
Instruction TLB
16 Bytes/cycle
Branch Predictor (BPU)
Instruction Fetch & PreDecode (16 B window)
MOP
Instruction Queue (50, 2x25 entries)
Macro-Fusion
64B/cycle
MicroCode Sequencer ROM (MS ROM)
5-Way Decode
Complex Decoder
Simple Decoder
1-4 µOPs
µOP
Stack Engine (SE)
Adder
4 µOPs
5 µOPs
Decoded Stream Buffer (DSB) (µOP Cache) (1.5k µOPs; 8-Way) (64 B window)
6 µOPs
MUX
Loop Stream Detector (LSD)
Allocation Queue (IDQ) (128, 2x64 µOPs)
Micro-Fusion
Register Alias Table (RAT)
4 µOP
Branch Order Buffer (BOB) (48-entry)
Load
FP
Int Vect
Int
Store
Common Data Buses (CDBs)
Move Elimination
Rename / Allocate / Retirement
ReOrder Buffer (224 entries)
Ones Idioms
Zeroing Idioms
Integer Physical Register File (180 Registers)
Scheduler
Unified Reservation Station (RS)
(97 entries)
Vector Physical Register File (168 Registers)
Port 0
Port 1
Port 5
Port 6
Port 2
Port 3
Port 4
Port 7
INT ALU
INT DIV
INT Vect ALU
INT Vect MUL
FP FMA
AES
Vect String
FP DIV
Branch
INT MUL
Bit Scan
Vect Shuffle
LEA
AGU
Load Data
Store Data
256bit/cycle
EUs
Execution Engine
Unified STLB
L2 Cache 256KiB 4-Way
32B/cycle
To L3
Store Buffer & Forwarding (56 entries)
Load Buffer (72 entries)
L1 Data Cache 32KiB 8-Way
Data TLB
Line Fill Buffers (LFB) (10 entries)
Memory Subsystem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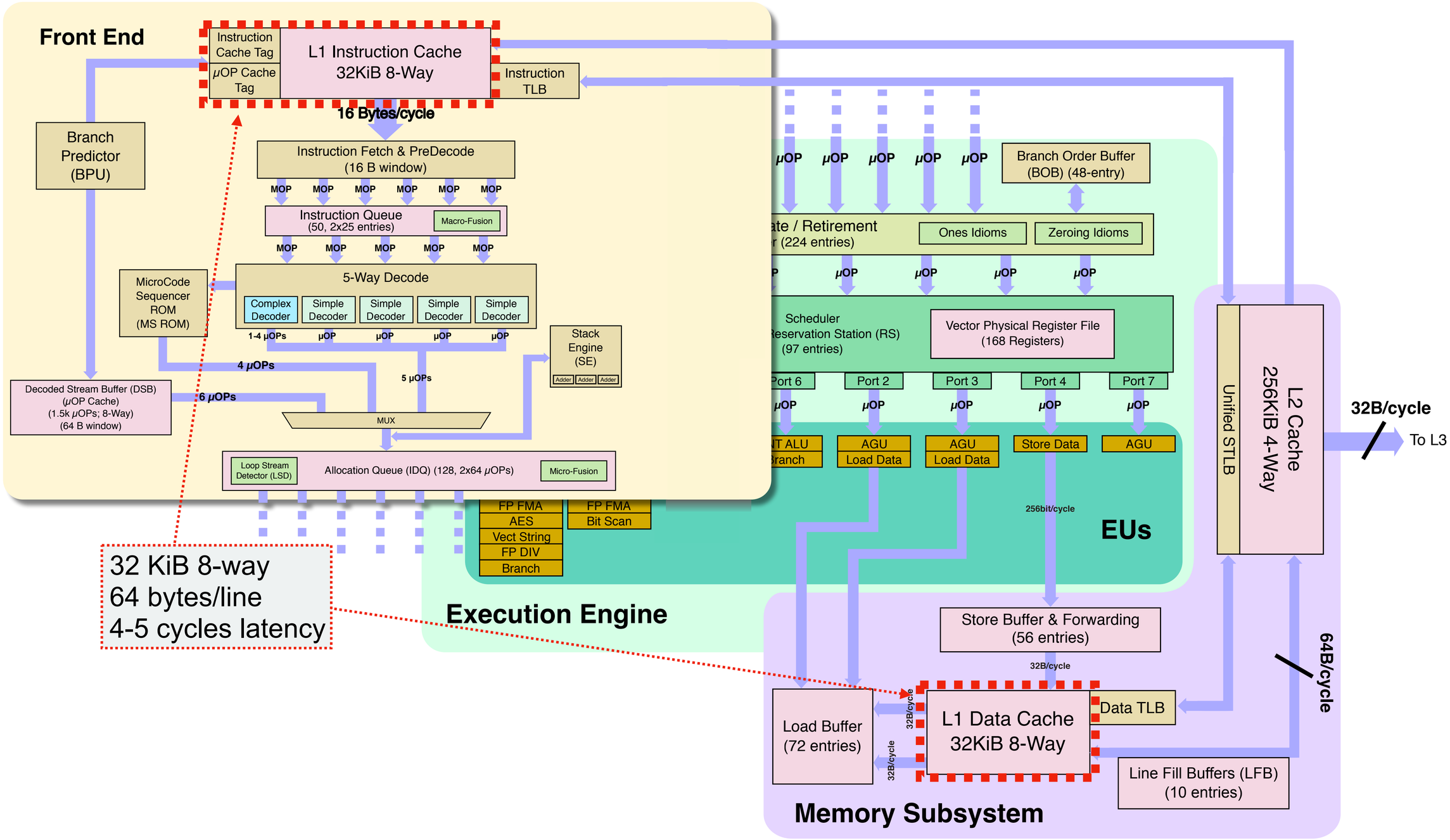
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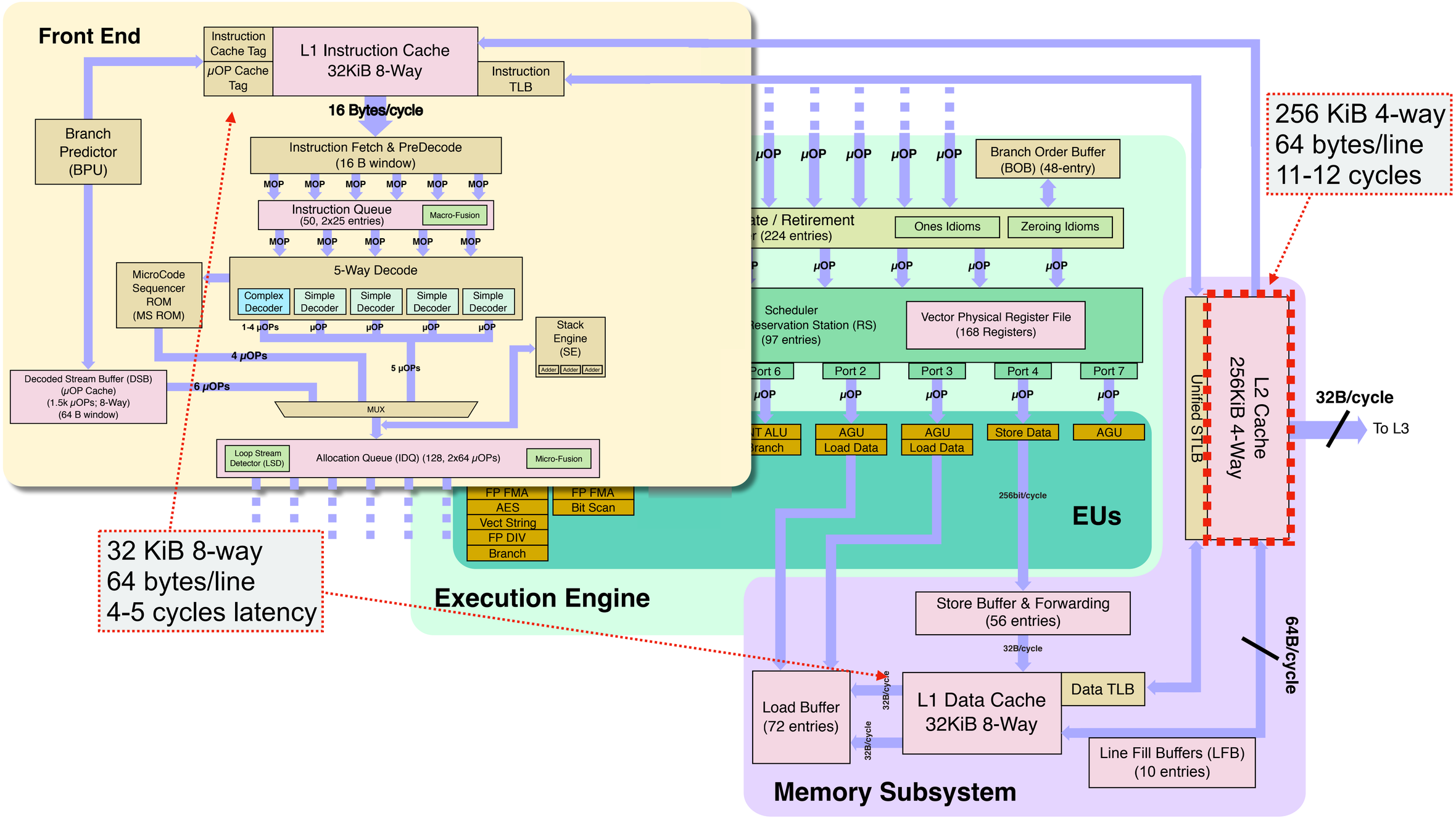
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64 bytes/line
11-12 cycles
L2 Cache
256KiB 4-Way
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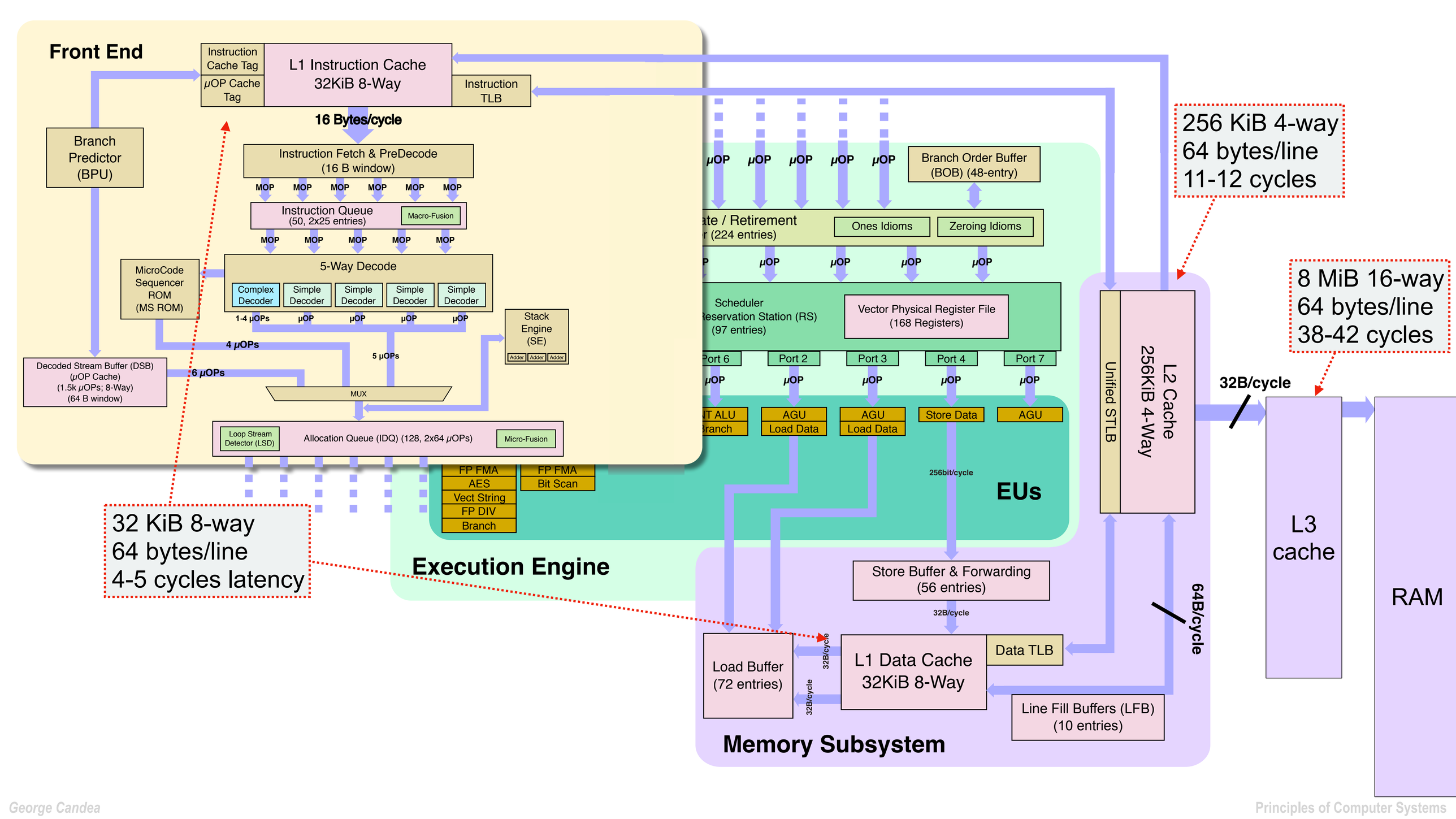
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38-42 cycles
32B/cycle
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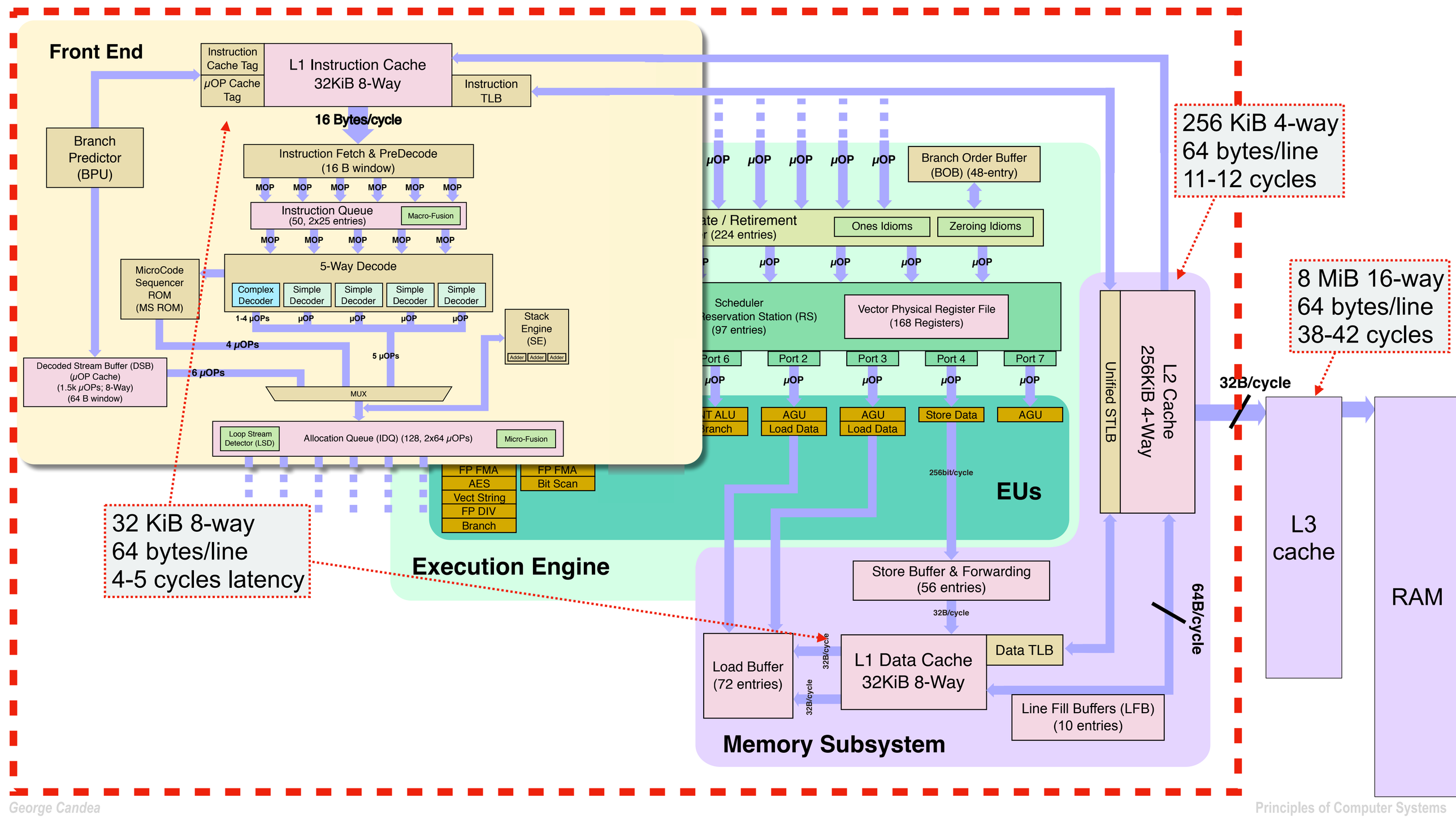
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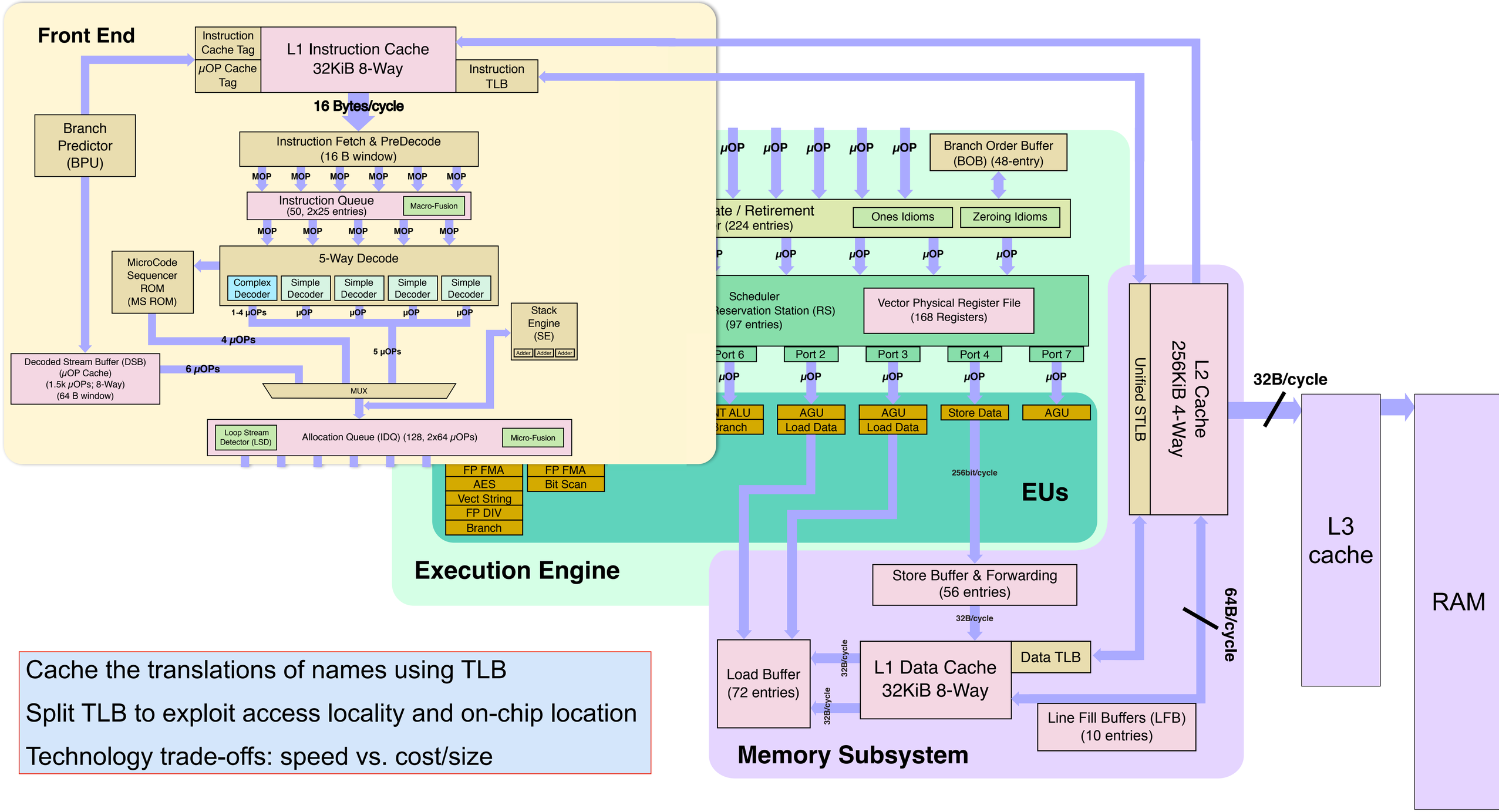
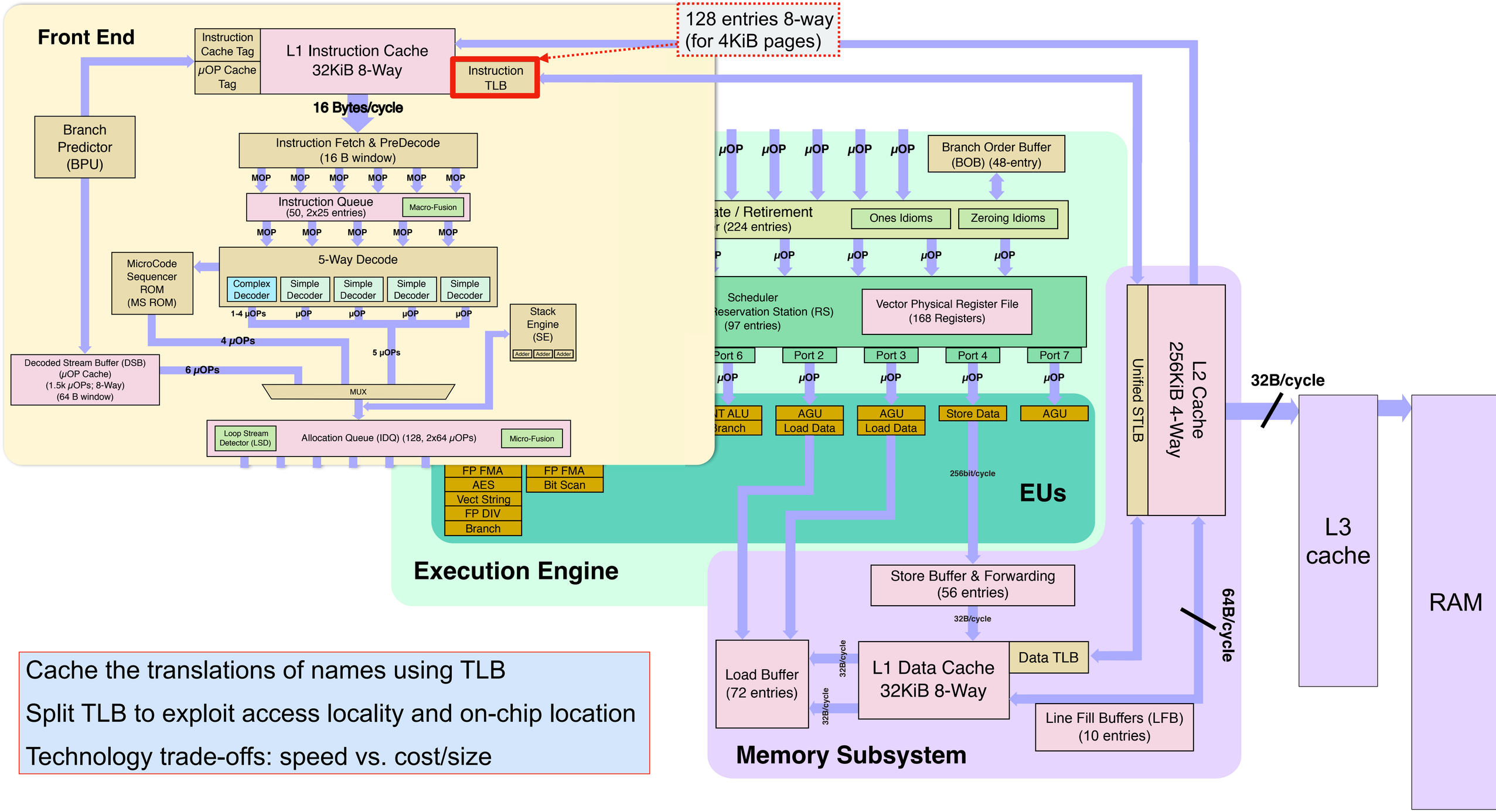
Zeroing Idioms
Scheduler
Reservation Station (RS)
(97 entries)
Vector Physical Register File
(168 Registers)
Port 6
Port 2
Port 3
Port 4
Port 7
AGU
Load Data
Store Data
FP FMA
AES
Vect String
FP DIV
Branch
FP FMA
Bit Scan
256bit/cycle
EUs
Execution Engine
256 KiB 4-way
64 bytes/line
11-12 cycles
Unified STLB
L2 Cache
256KiB 4-Way
32B/cycle
8 MiB 16-way
64 bytes/line
38-42 cycles
L3 cache
RAM
Store Buffer & Forwarding (56 entries)
32B/cycle
Load Buffer (72 entries)
L1 Data Cache 32KiB 8-Way
Data TLB
Line Fill Buffers (LFB) (10 entries)
64B/cycle
Memory Subsystem



Cache the translations of names using TLB

Split TLB to exploit access locality and on-chip location

Technology trade-offs: speed vs. cost/size



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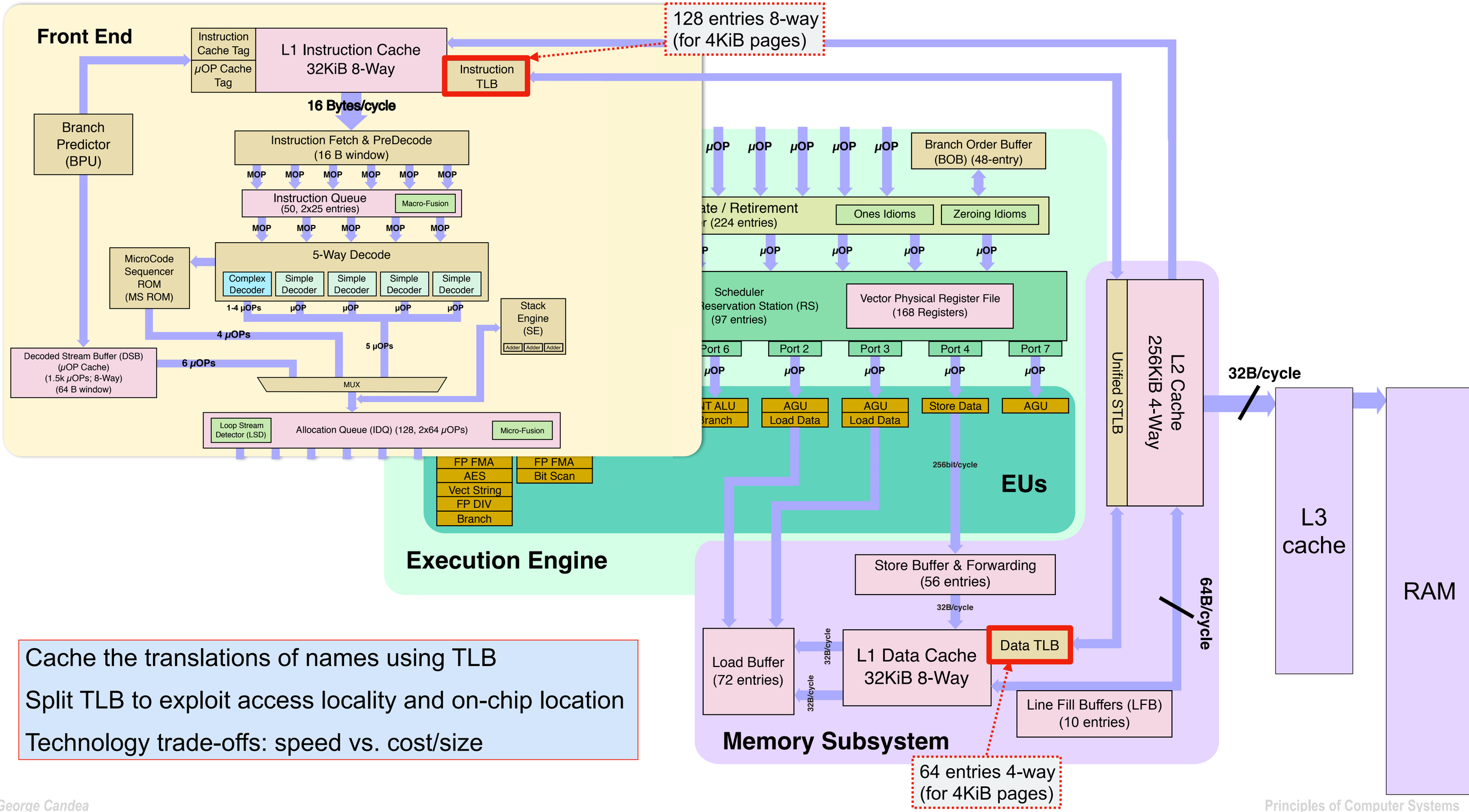

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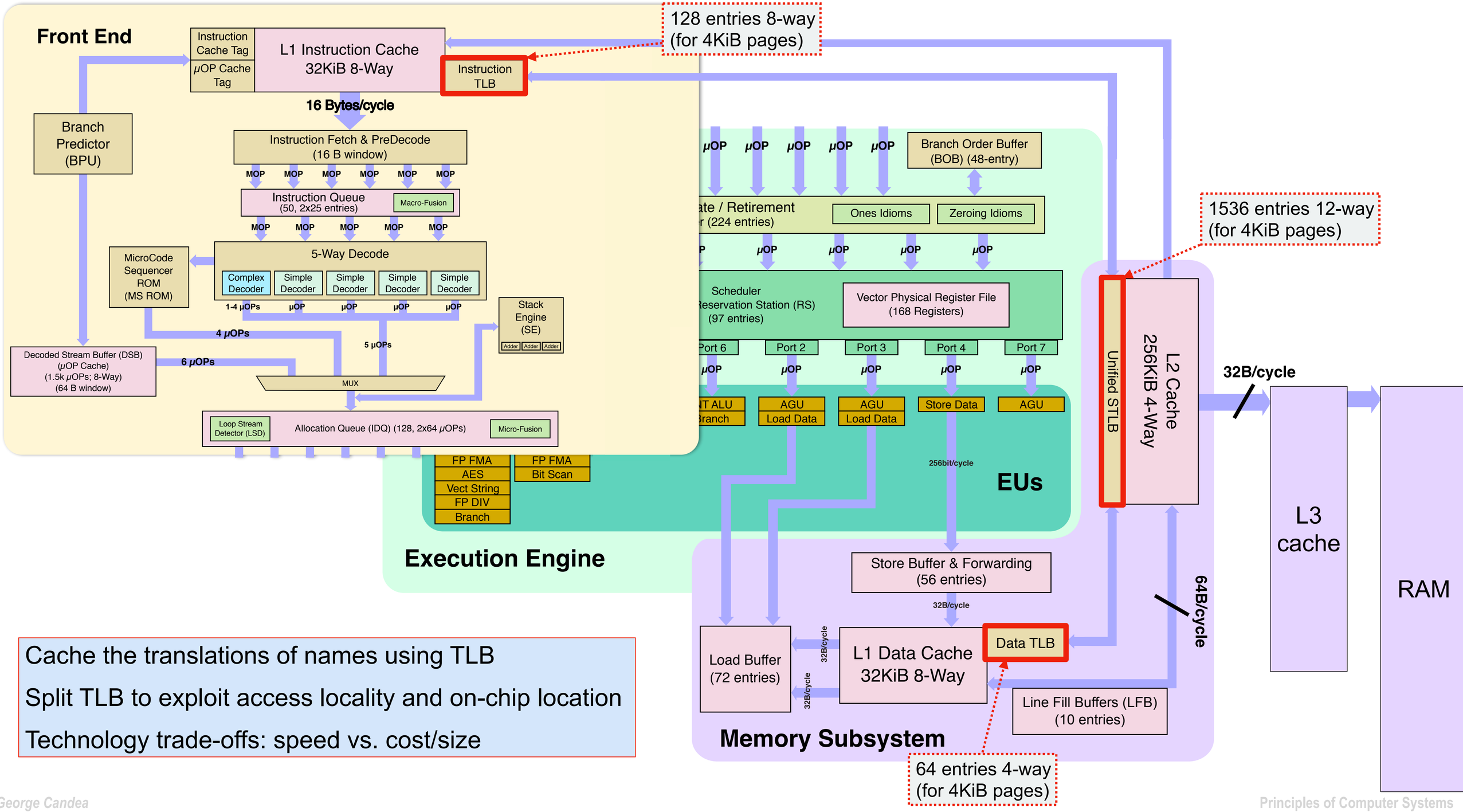

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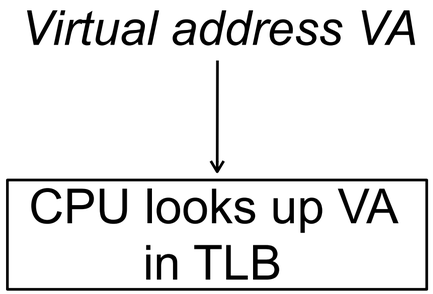
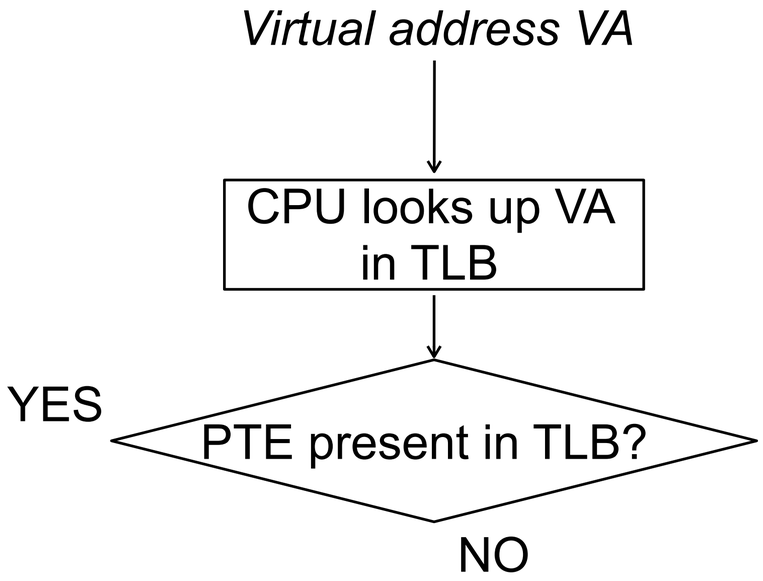
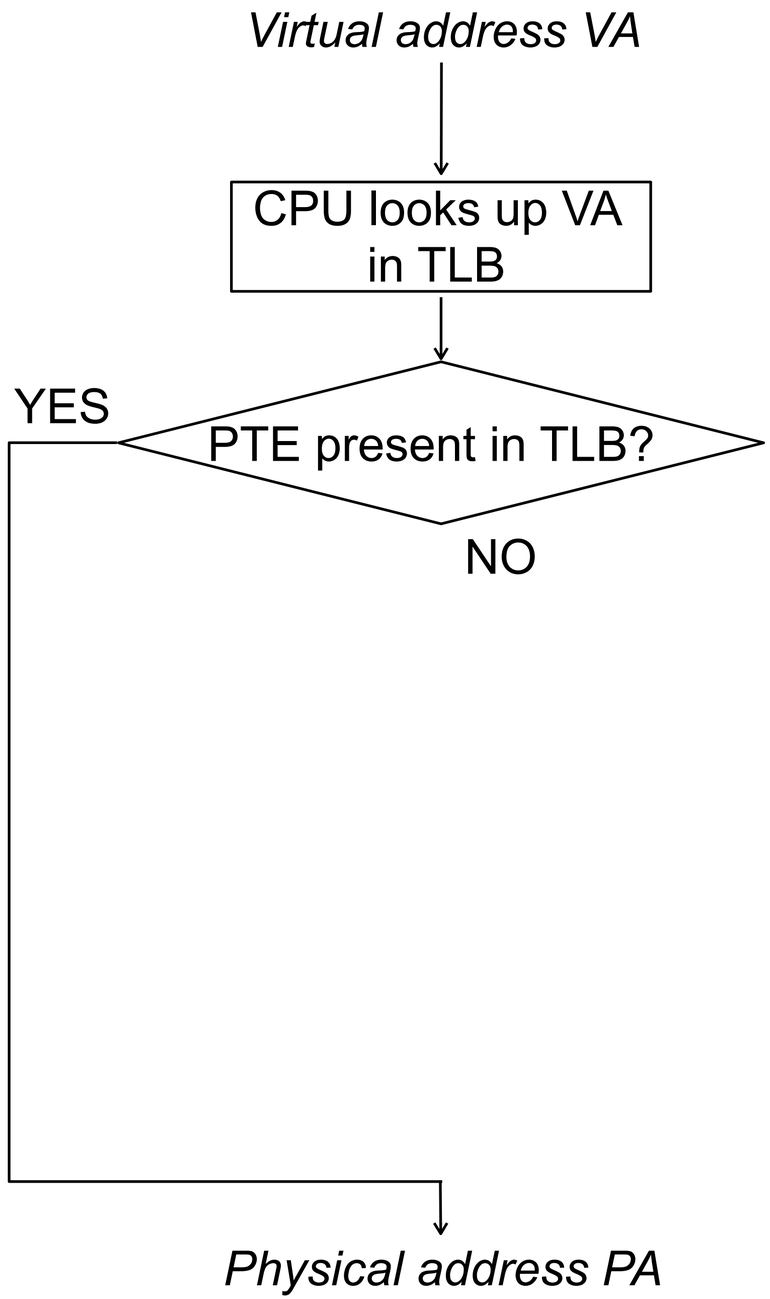
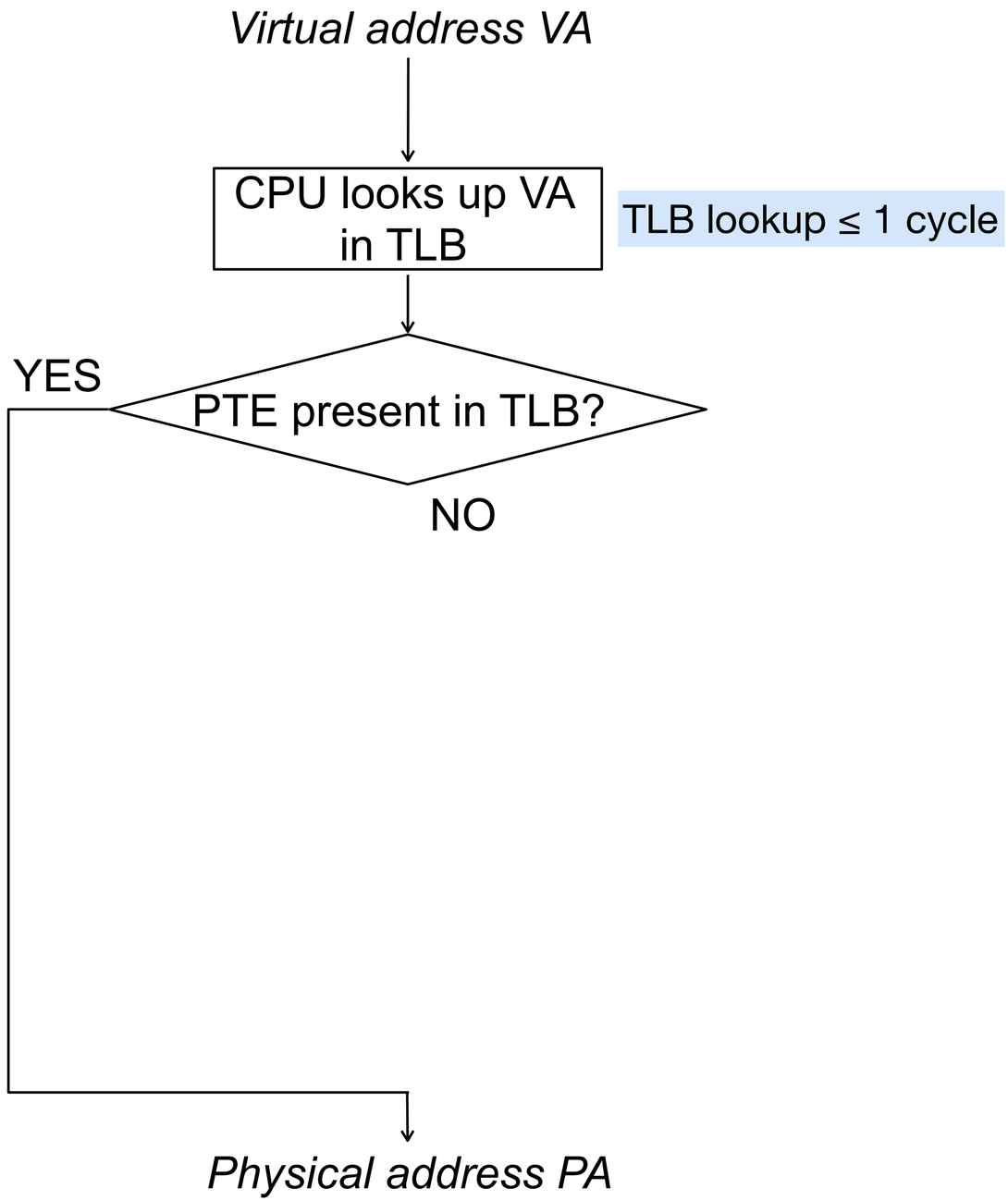
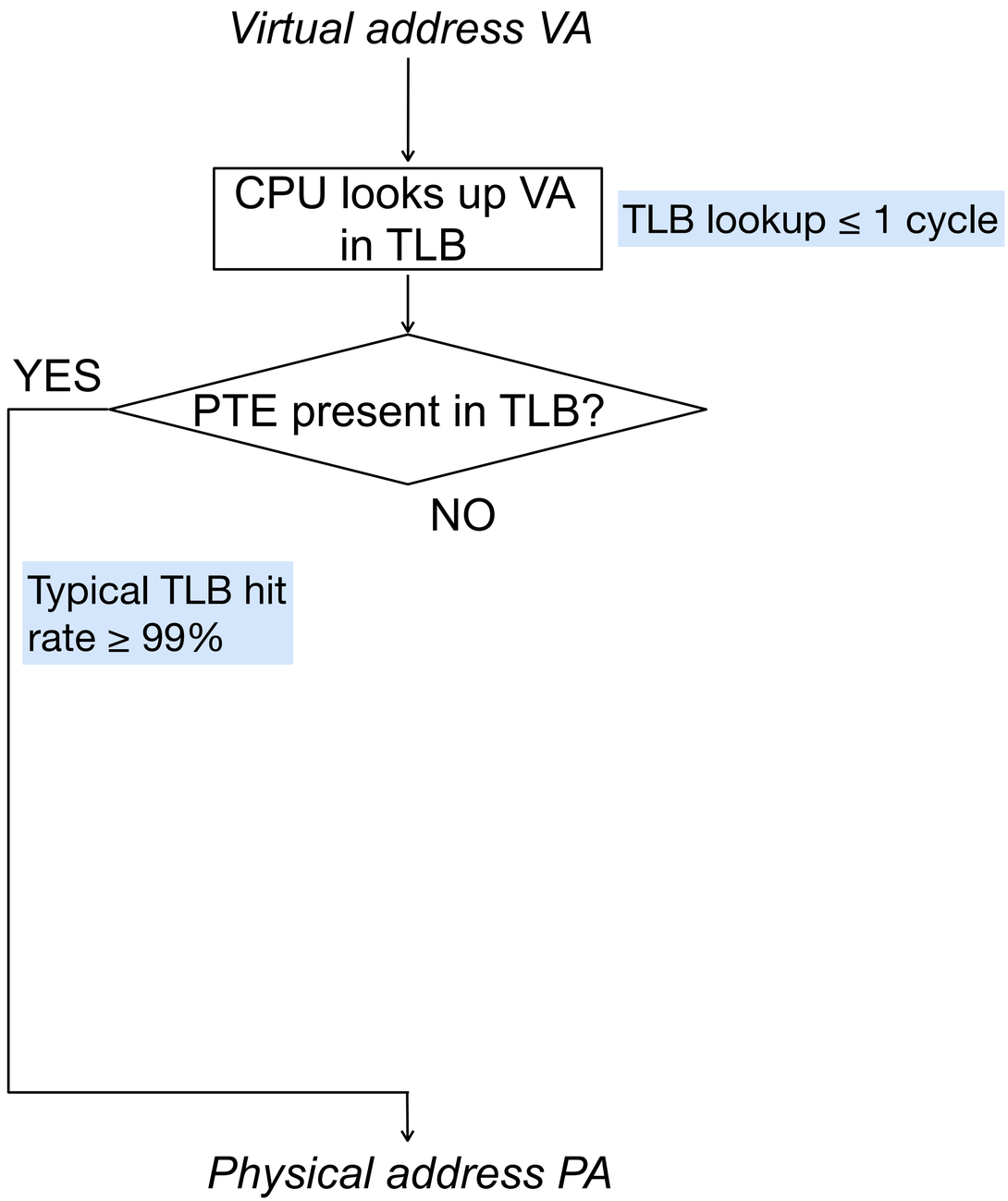
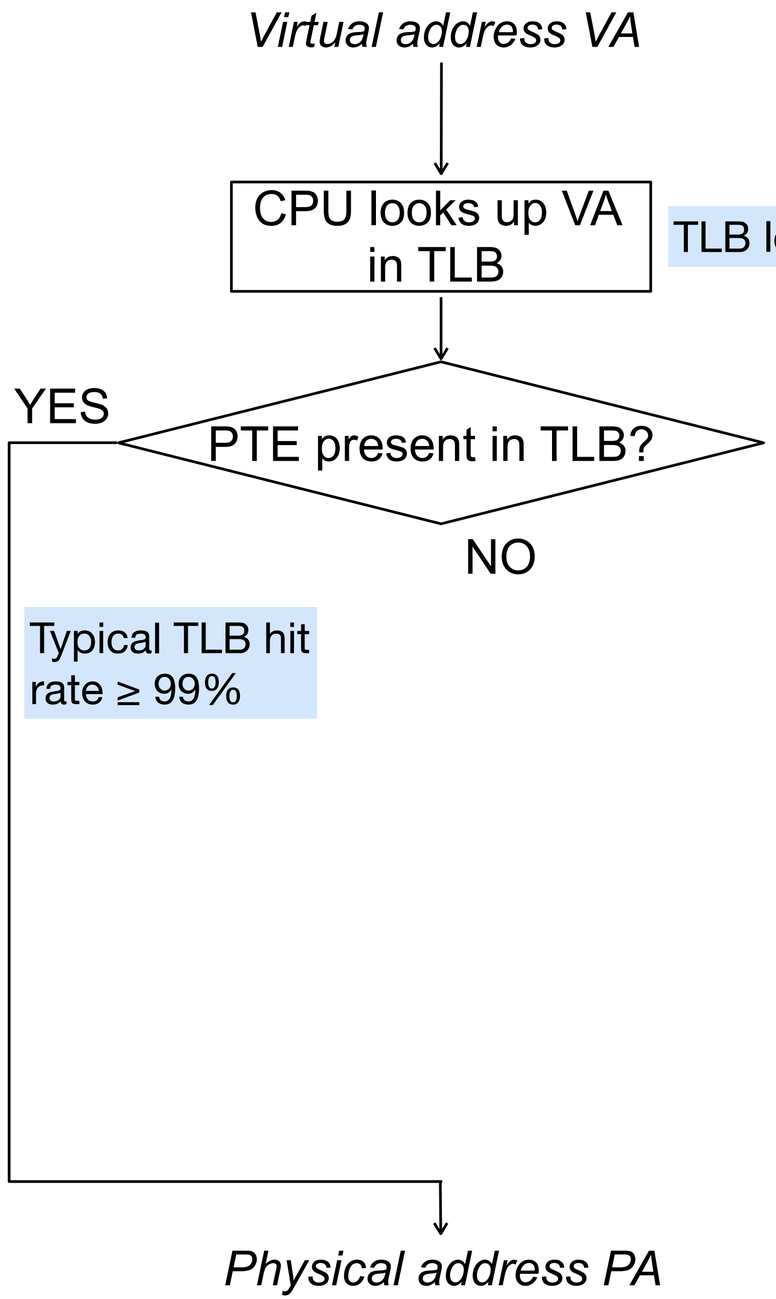

Virtual address VA
CPU looks up VA
in TLB


Virtual address VA
CPU looks up VA in TLB
PTE present in TLB?
YES
NO

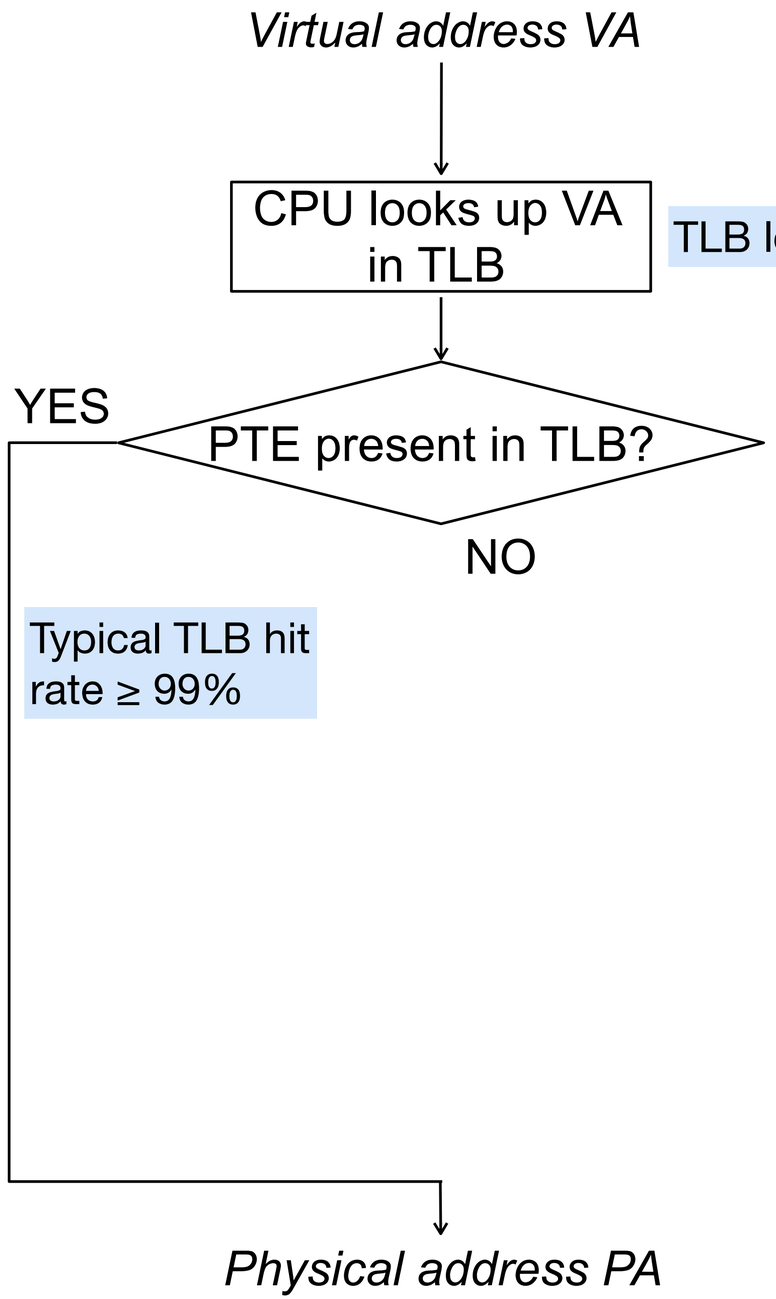

Virtual address VA
CPU looks up VA in TLB
PTE present in TLB?
YES
NO
Physical address PA


Virtual address VA
CPU looks up VA in TLB
TLB lookup ≤ 1 cycle
PTE present in TLB?
YES
NO
Physical address PA

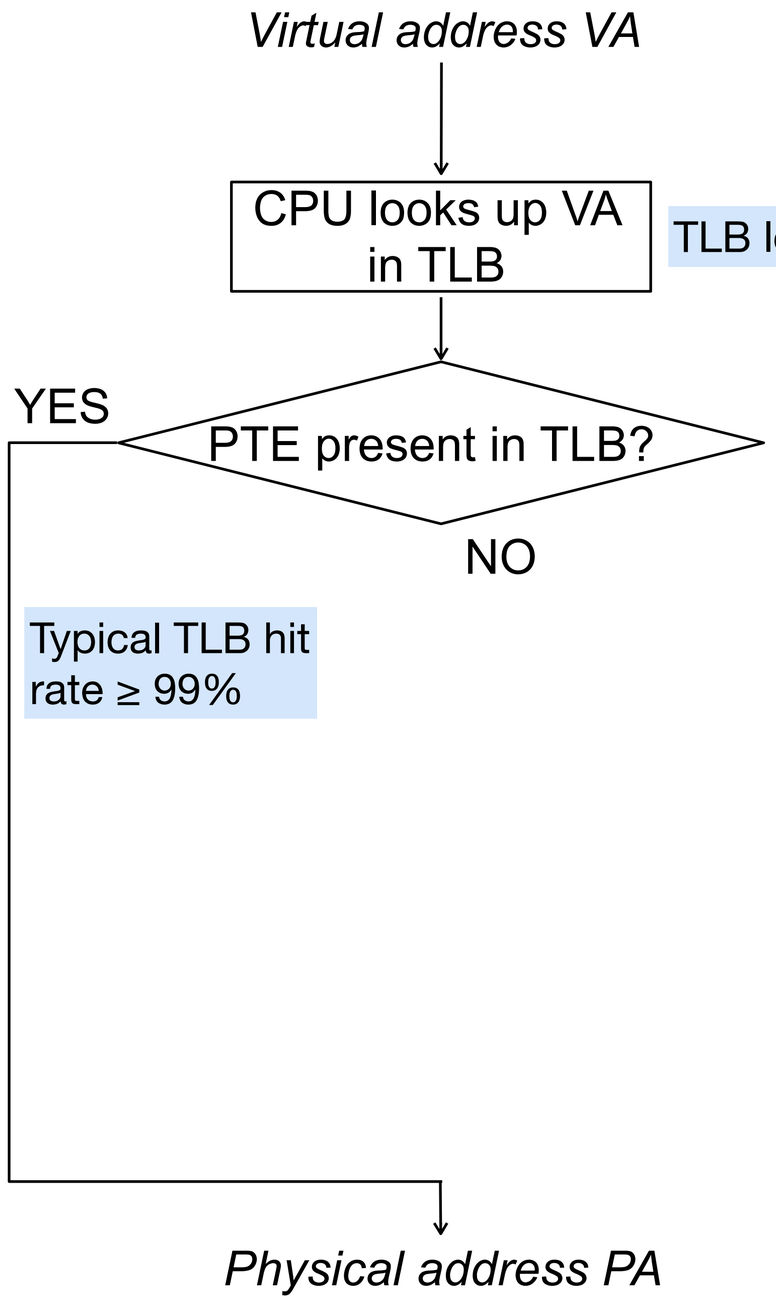

Virtual address VA
CPU looks up VA in TLB
TLB lookup ≤ 1 cycle
PTE present in TLB?
YES
NO
Typical TLB hit rate ≥ 99%
Physical address PA



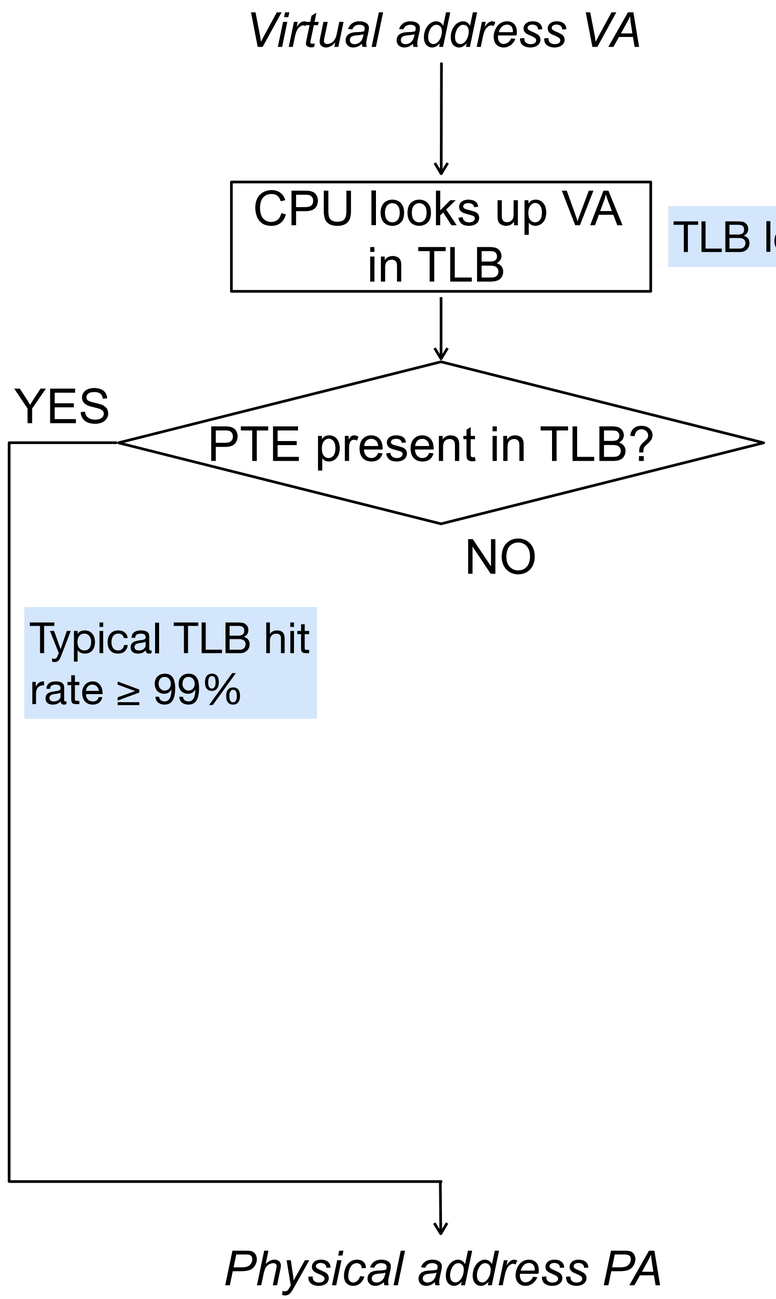
Read from L1 = ~4 cycles



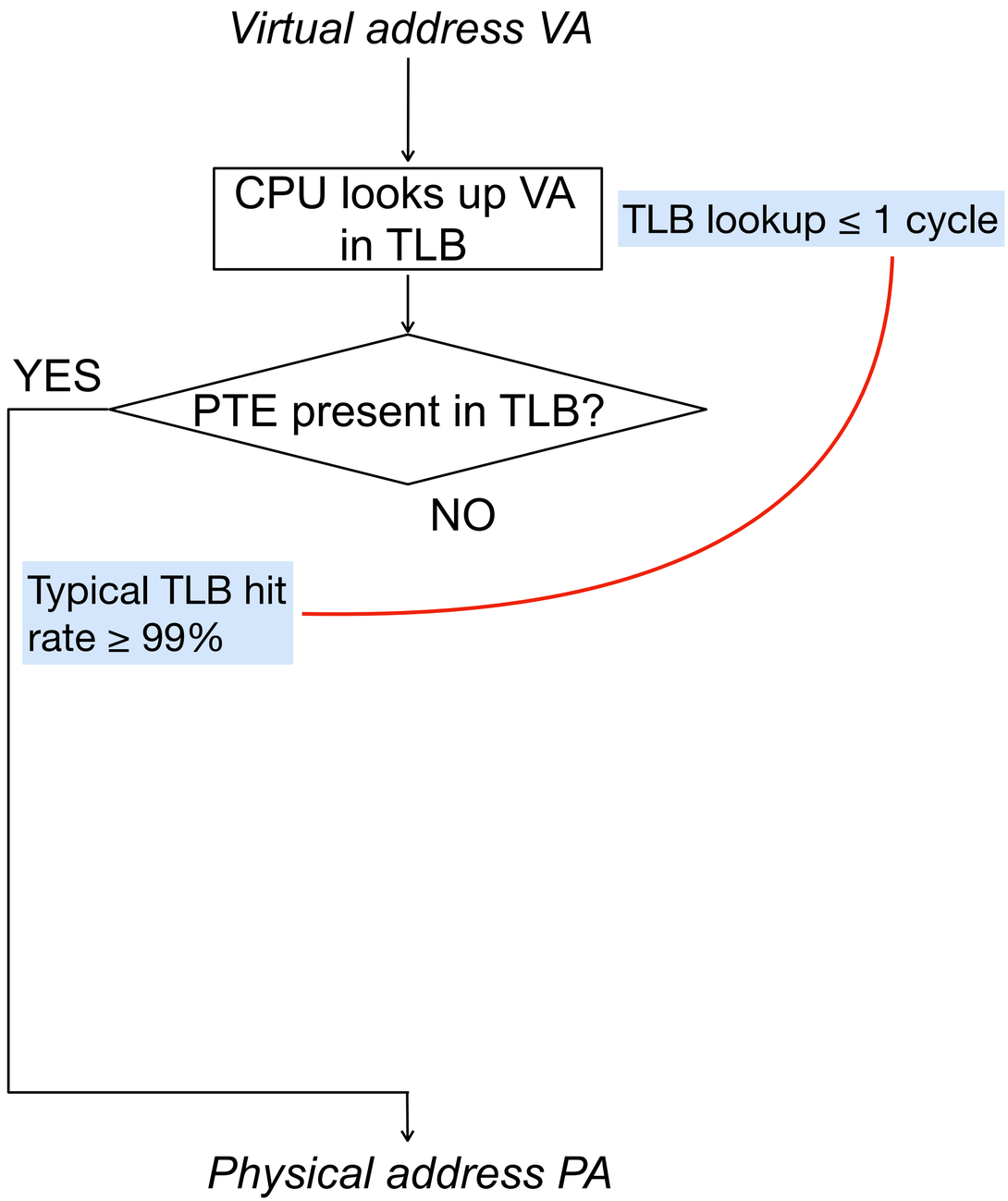
Read from L1 = ~4 cycles
Read from L2 = ~12 cycles



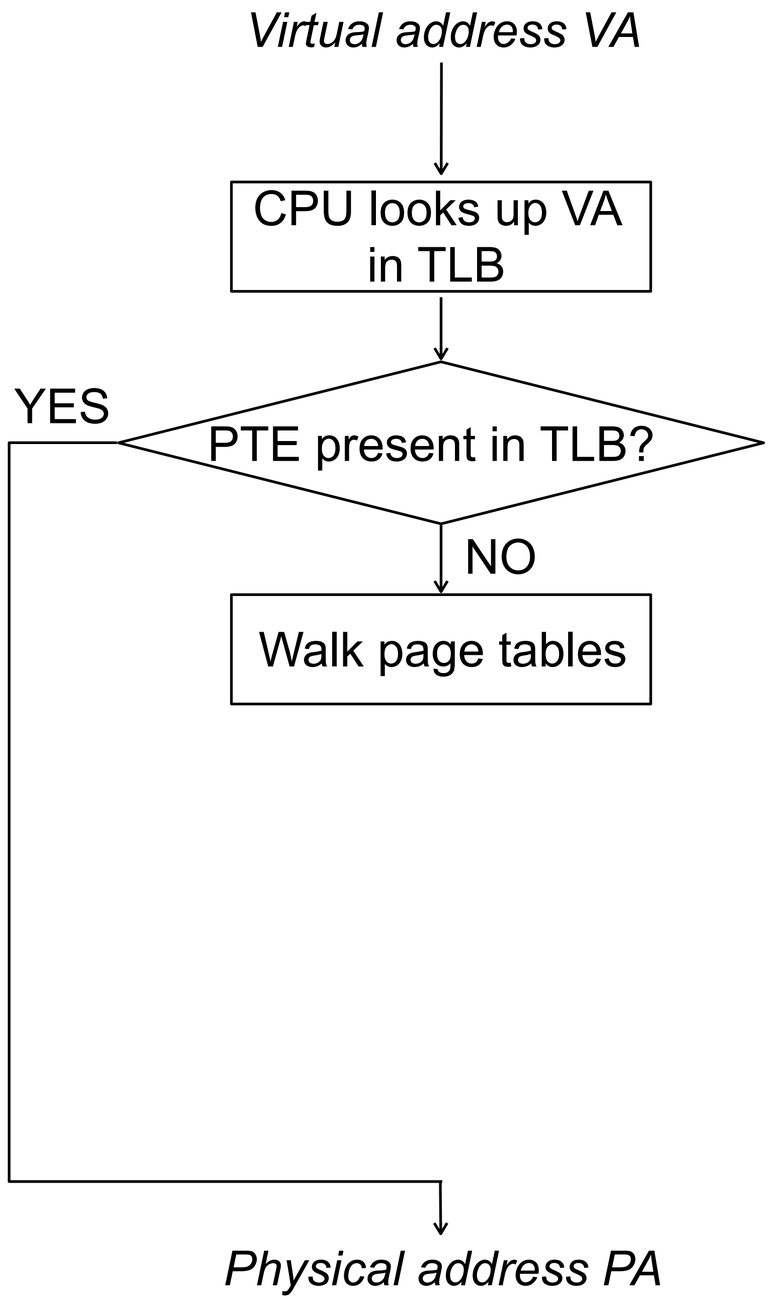
Read from L1 = ~4 cycles
Read from L2 = ~12 cycles
Read from L3 = ~30-40 cycles

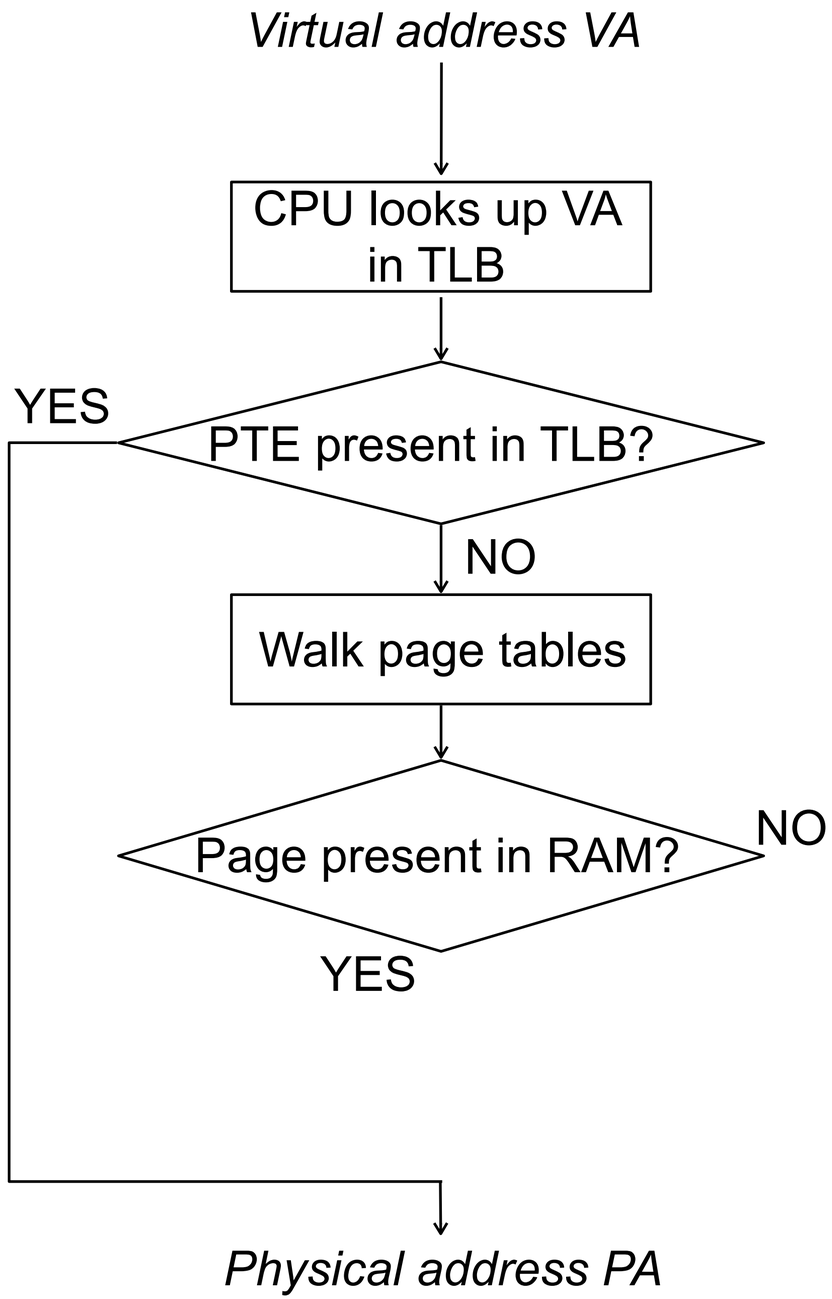


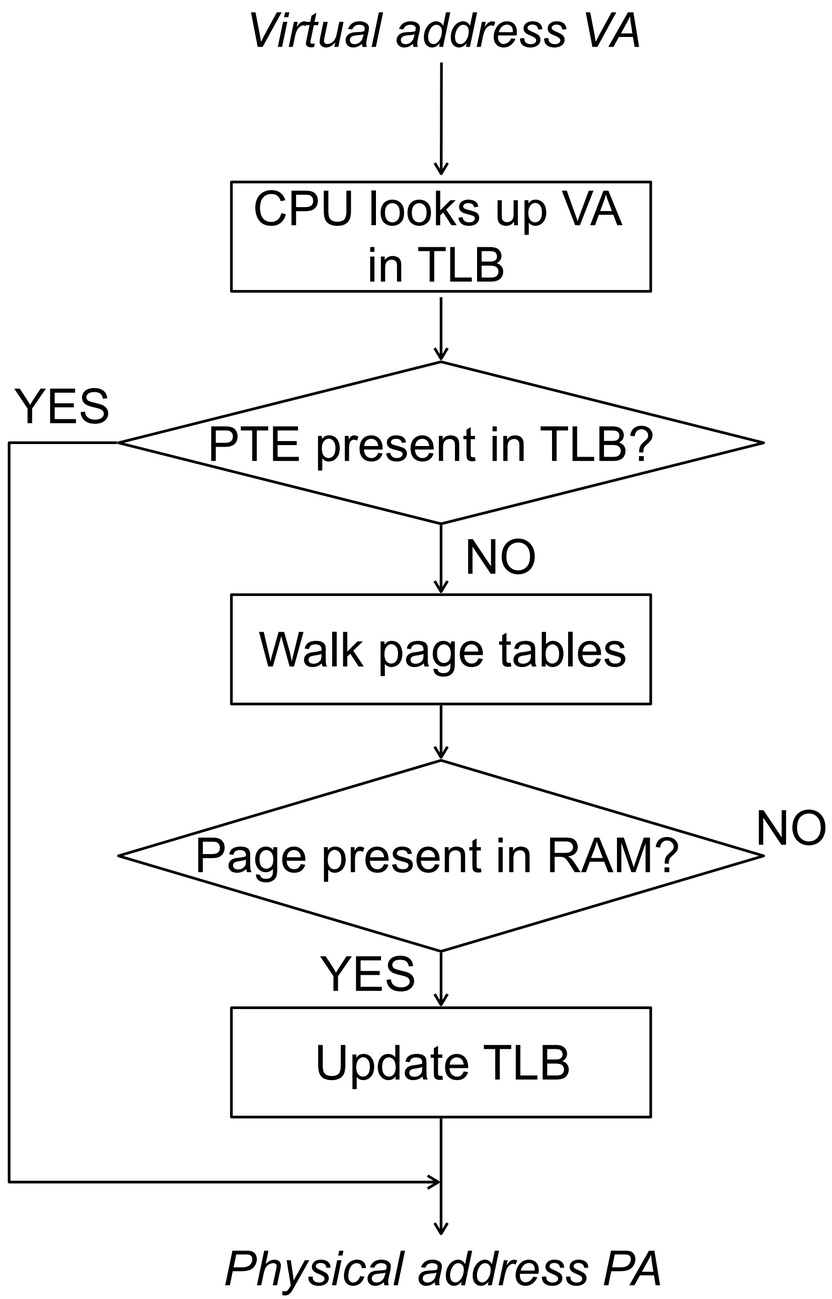
Read from L1 = ~4 cycles
Read from L2 = ~12 cycles
Read from L3 = ~30-40 cycles
Read from RAM = ~100-120 cycles

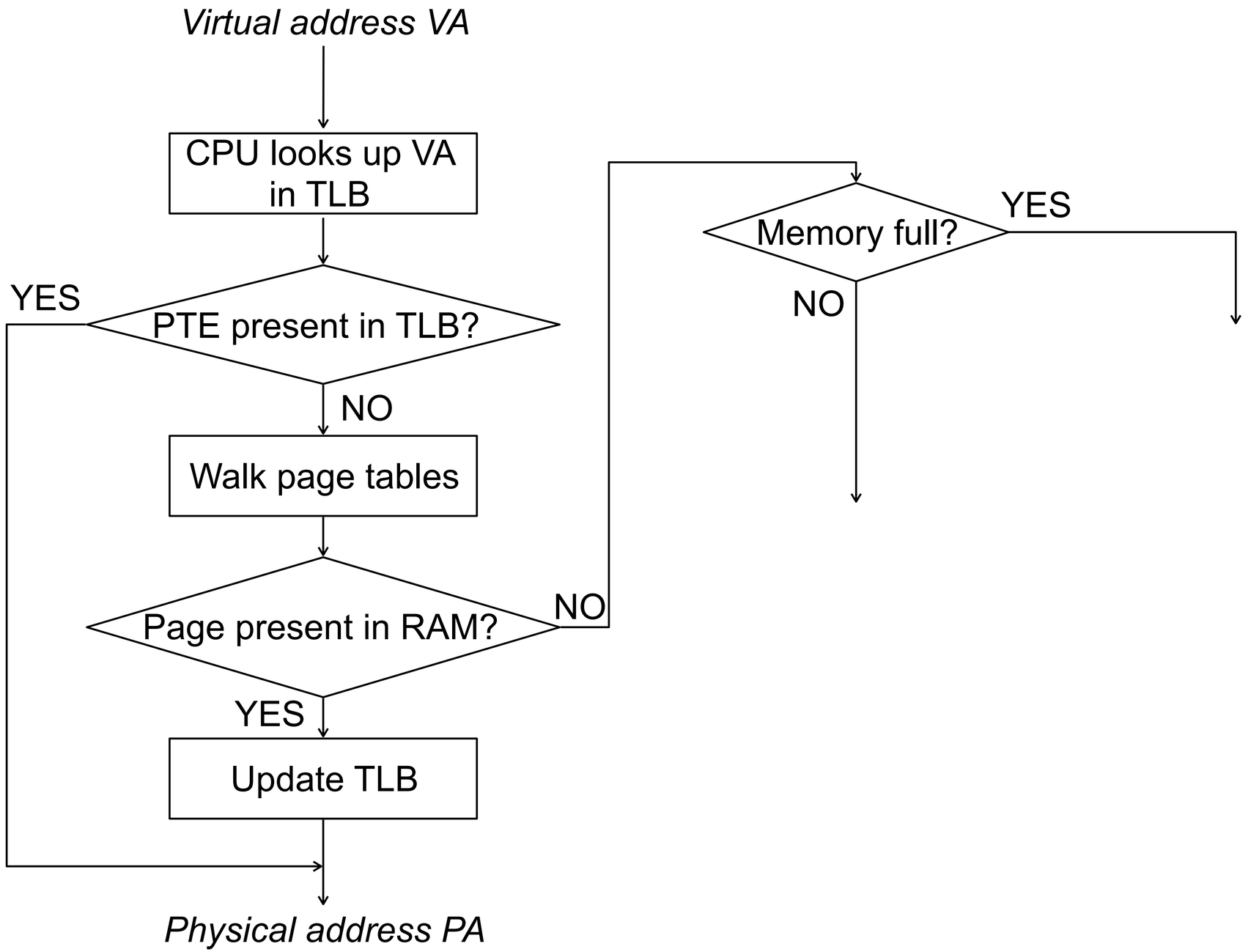


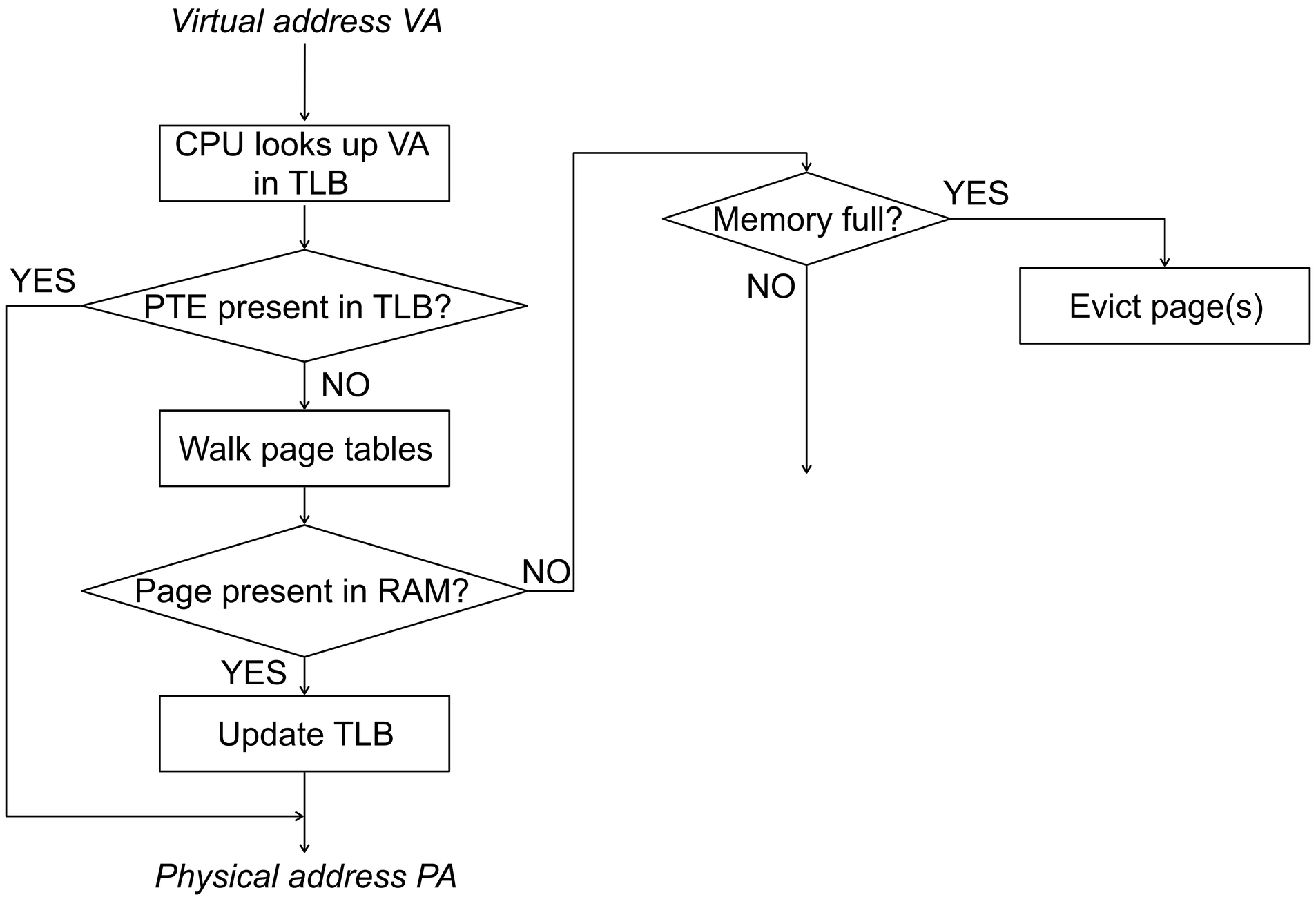
Read from L1 = ~4 cycles
Read from L2 = ~12 cycles
Read from L3 = ~30-40 cycles
Read from RAM = ~100-120 cycles

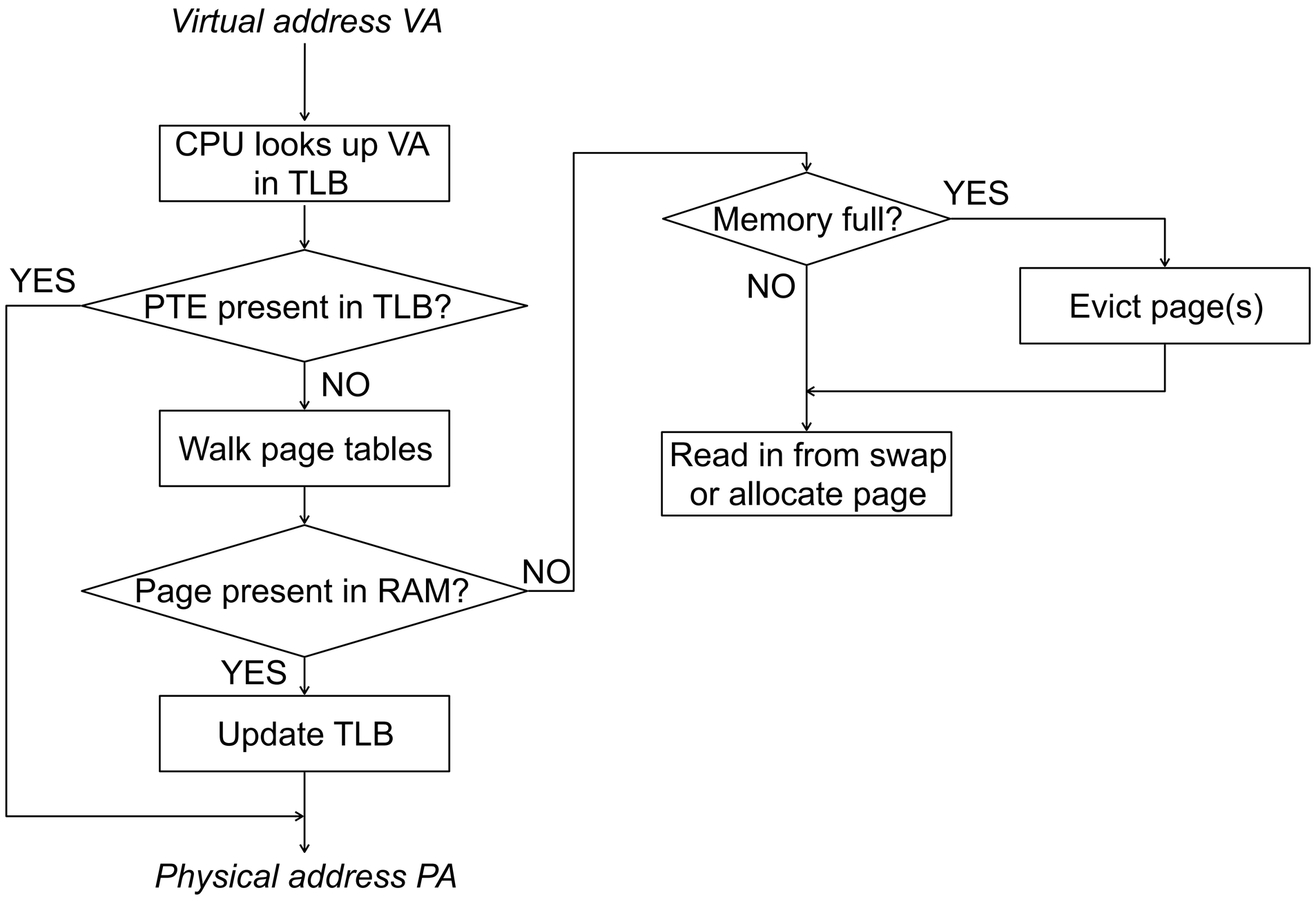

Virtual address VA
CPU looks up VA in TLB
PTE present in TLB?
YES
NO
Walk page tables
Physical address PA

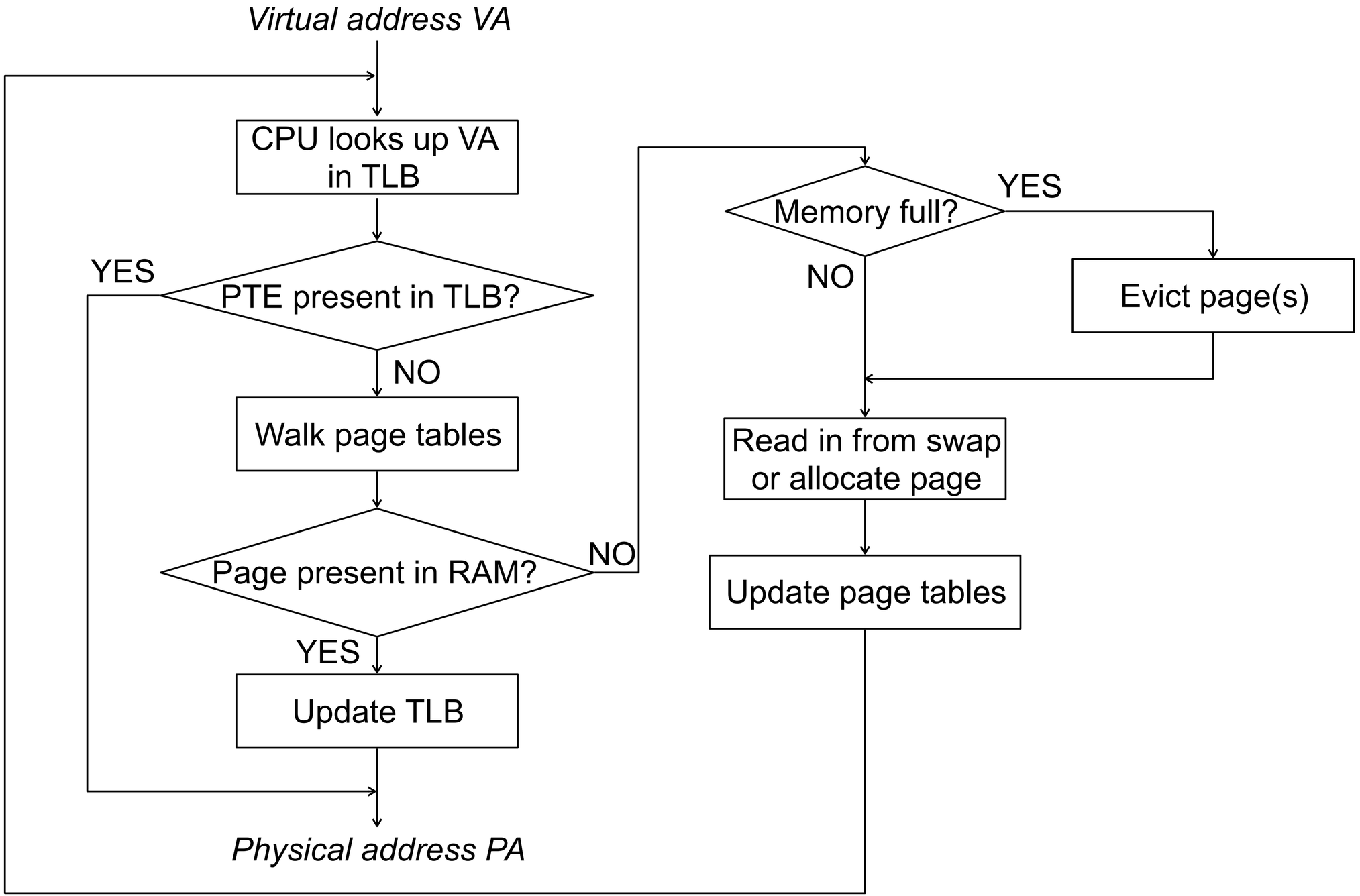

Virtual address VA
CPU looks up VA in TLB
PTE present in TLB?
YES
NO
Walk page tables
Page present in RAM?
NO
YES
Physical address PA

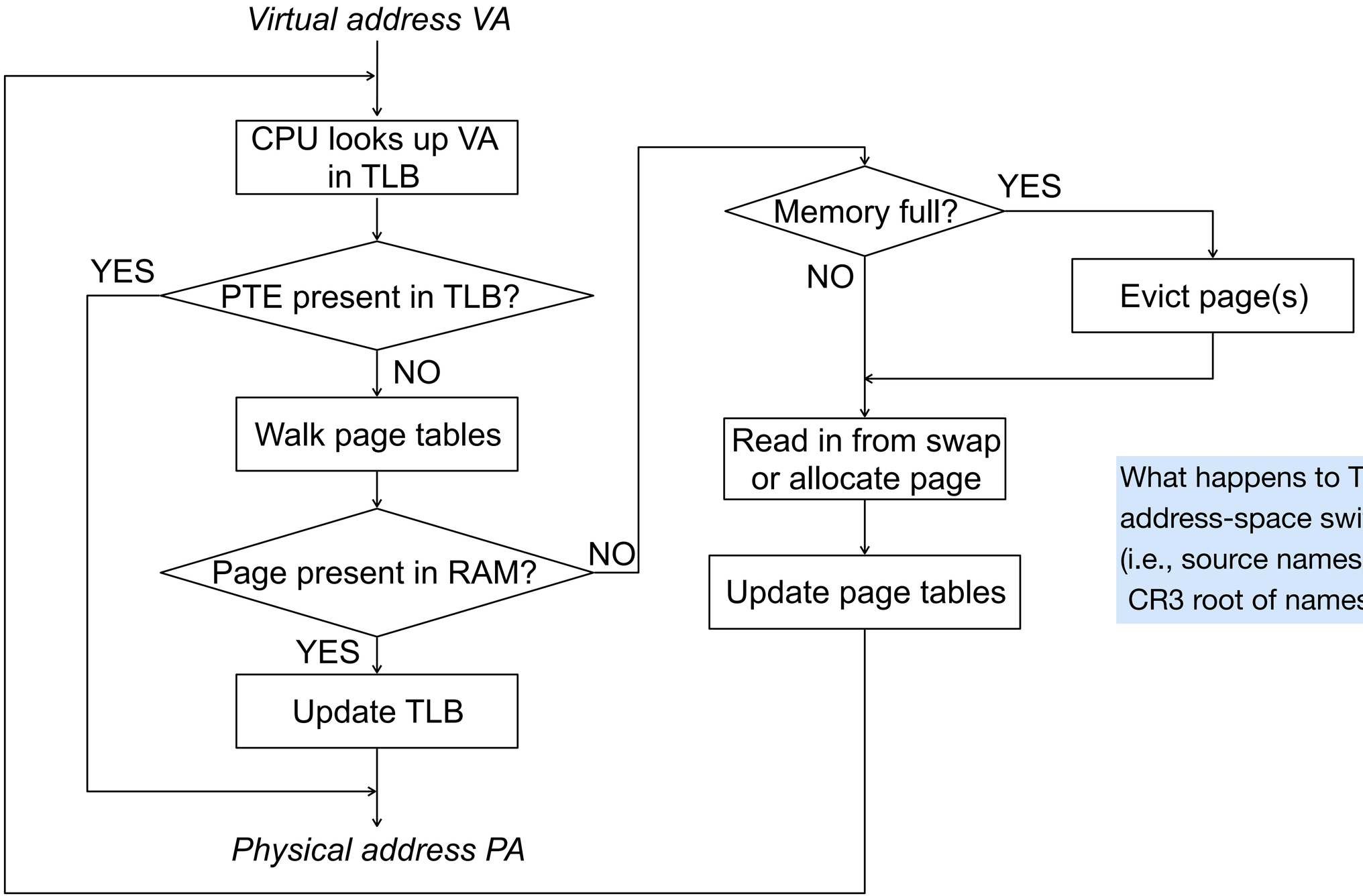

Virtual address VA
CPU looks up VA in TLB
PTE present in TLB?
YES
NO
Walk page tables
Page present in RAM?
NO
YES
Update TLB
Physical address PA


Virtual address VA
CPU looks up VA in TLB
PTE present in TLB?
YES
NO
Walk page tables
Page present in RAM?
NO
YES
Memory full?
YES
NO
Update TLB
Physical address PA

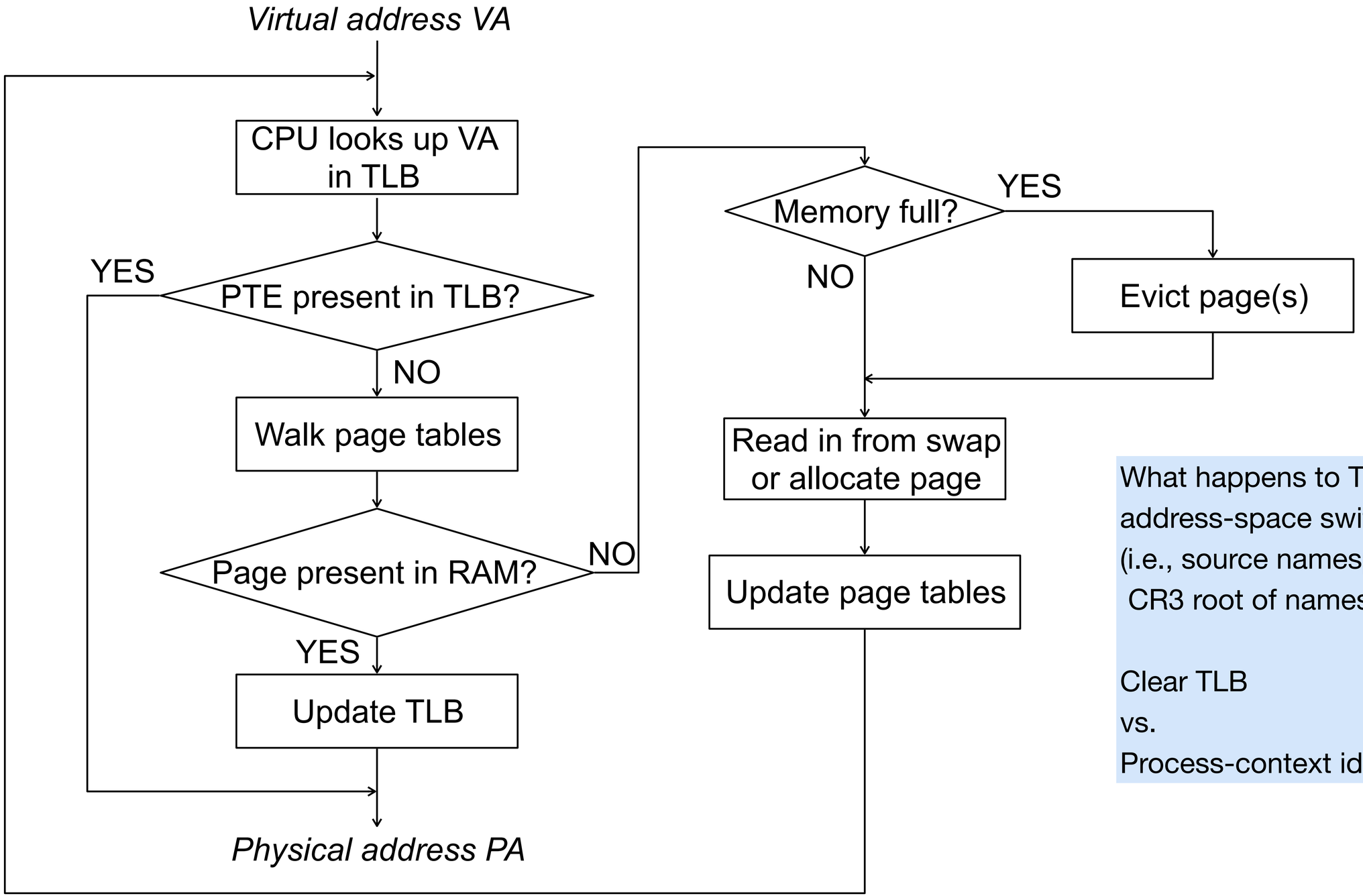

Virtual address VA
CPU looks up VA in TLB
PTE present in TLB?
YES
NO
Walk page tables
Page present in RAM?
NO
YES
Memory full?
YES
NO
Evict page(s)
Update TLB
Physical address PA


Virtual address VA
CPU looks up VA in TLB
PTE present in TLB?
YES
NO
Walk page tables
Page present in RAM?
NO
YES
Update TLB
Physical address PA
Memory full?
YES
NO
Evict page(s)
Read in from swap or allocate page


Virtual address VA
CPU looks up VA in TLB
PTE present in TLB?
YES
NO
Walk page tables
Page present in RAM?
NO
YES
Update TLB
Physical address PA
Memory full?
YES
NO
Evict page(s)
Read in from swap or allocate page
Update page tables

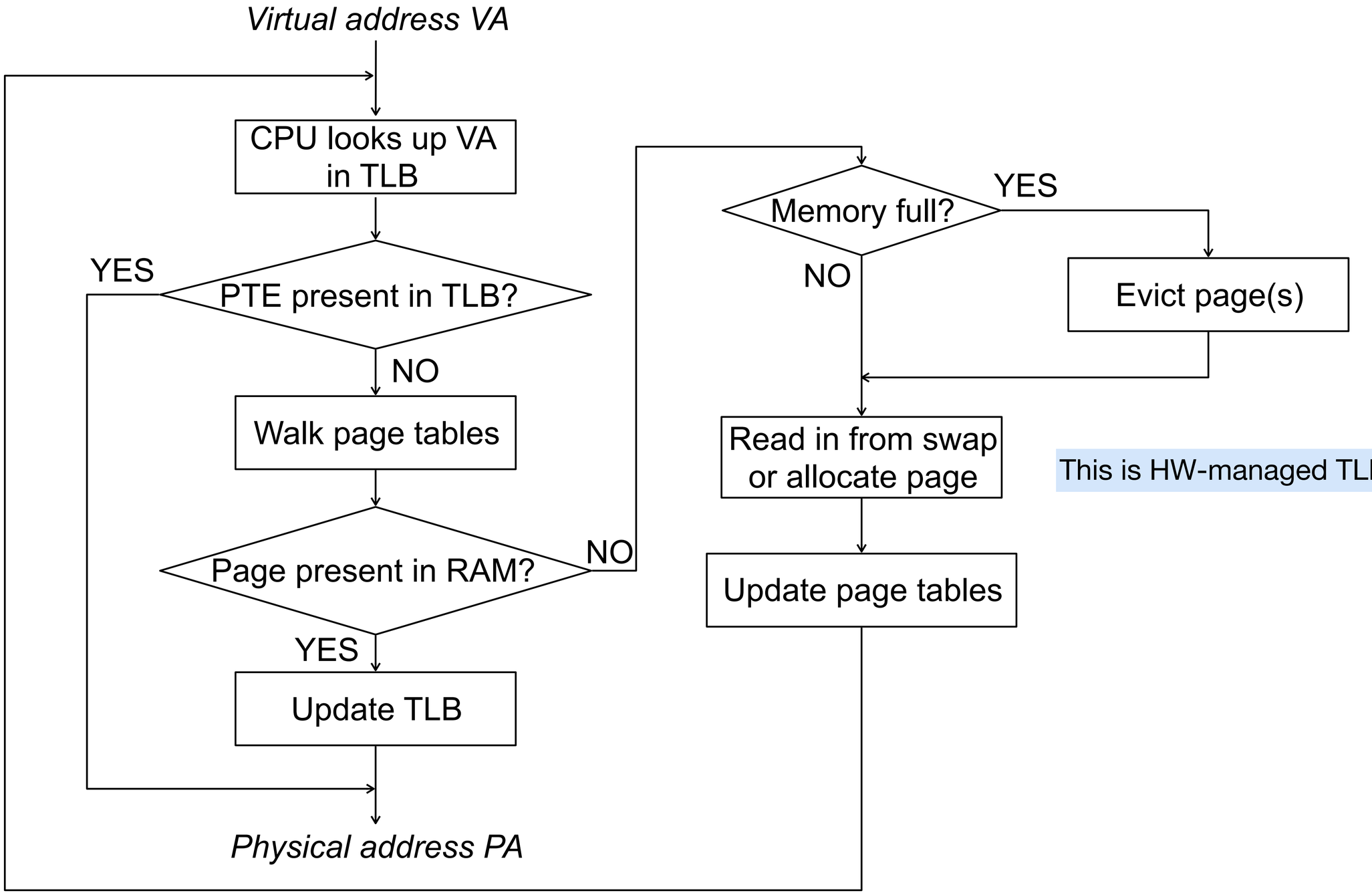


What happens to TLB on an address-space switch?
(i.e., source namespace differs => CR3 root of namespace changes)

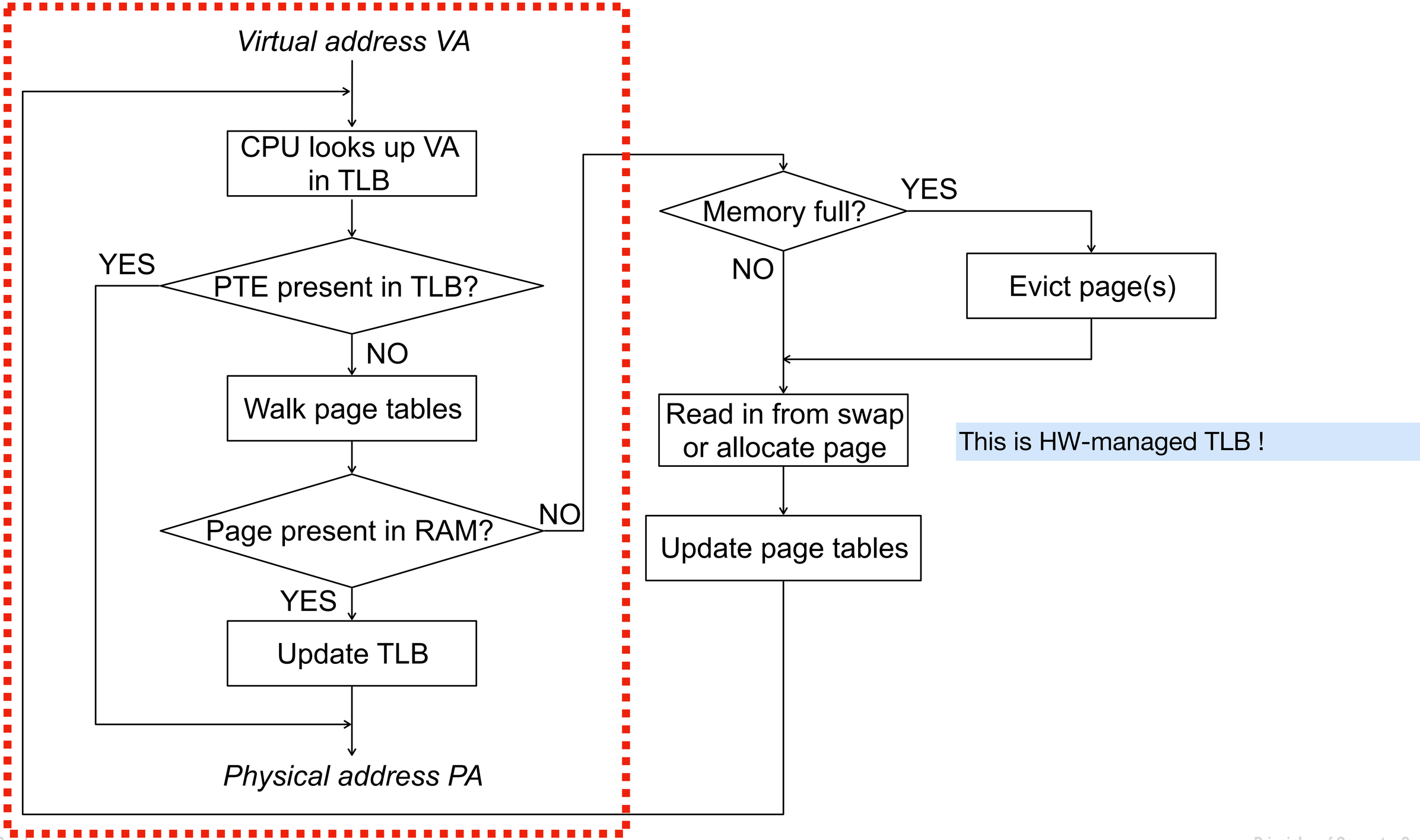


What happens to TLB on an address-space switch?
(i.e., source namespace differs => CR3 root of namespace changes)

Clear TLB
vs.
Process-context identifier (PCID)



This is HW-managed TLB !



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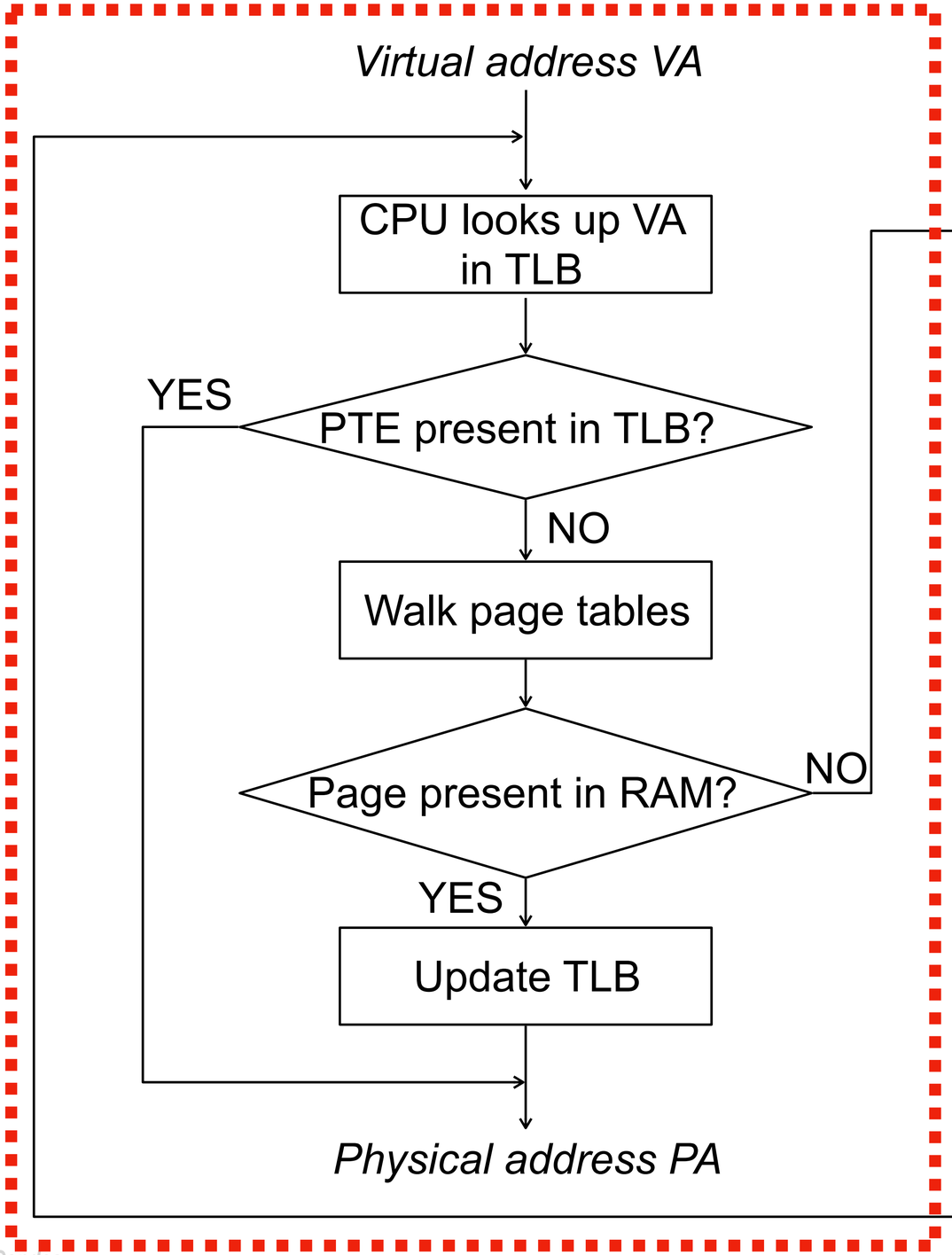
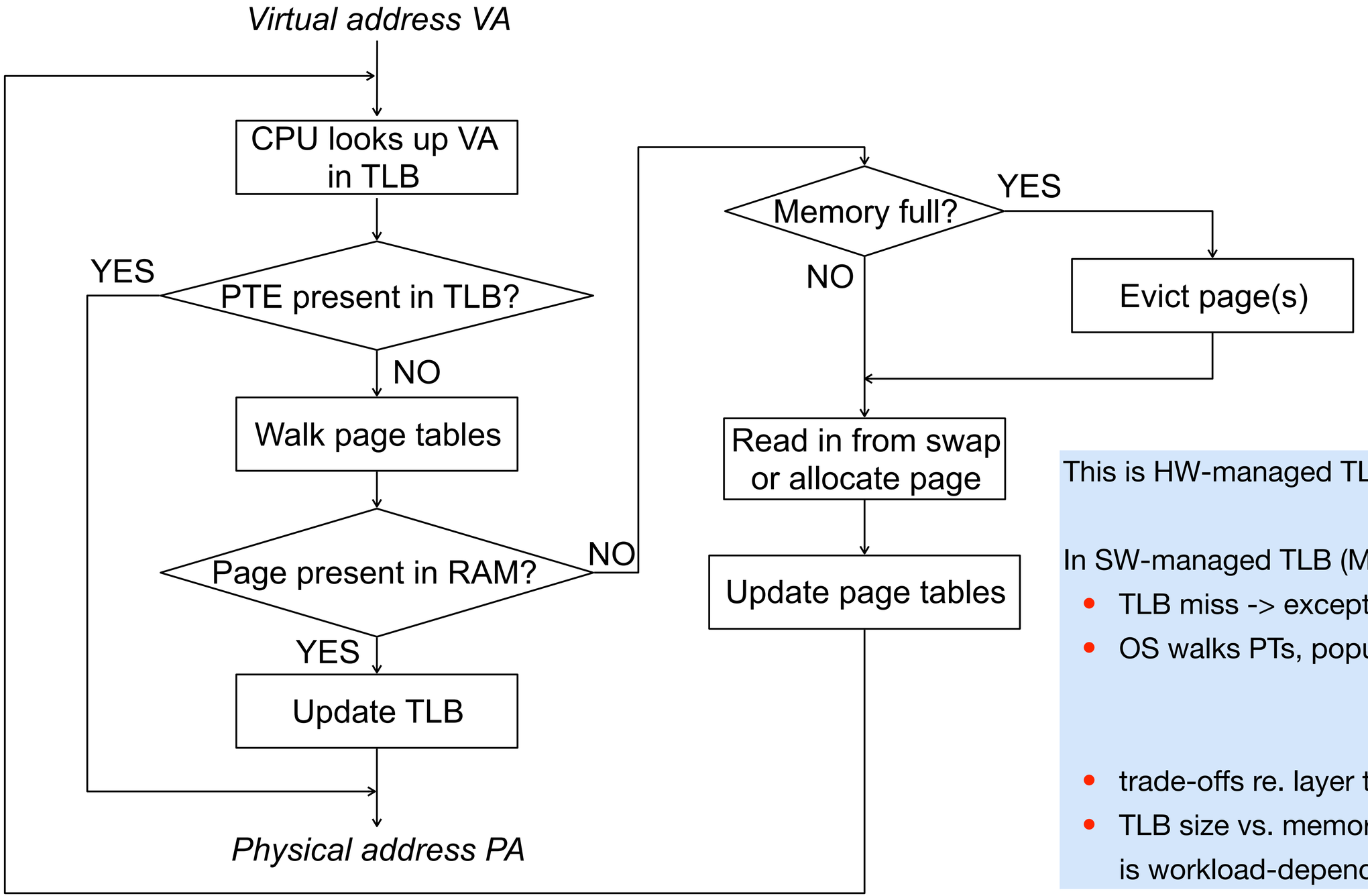


This is HW-managed TLB !

In SW-managed TLB (MIPS, SPARC, …)

- TLB miss -> exception to OS
- OS walks PTs, populates TLB



This is HW-managed TLB !

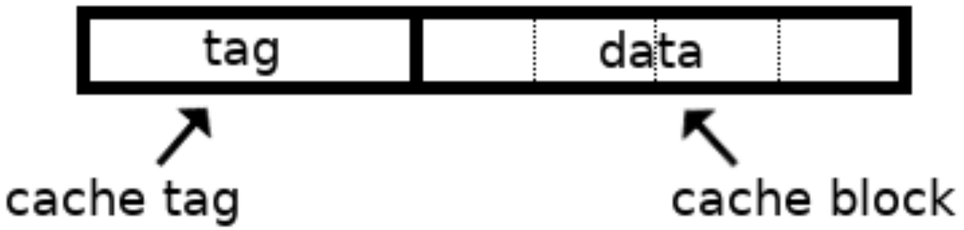
In SW-managed TLB (MIPS, SPARC, …)

- TLB miss -> exception to OS
- OS walks PTs, populates TLB

- trade-offs re. layer to delegate to
- TLB size vs. memory size trade-off is workload-dependent => hard!

Cache structure

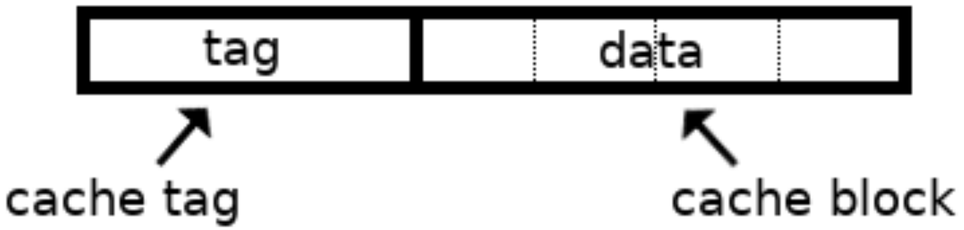
Cache entry (line)



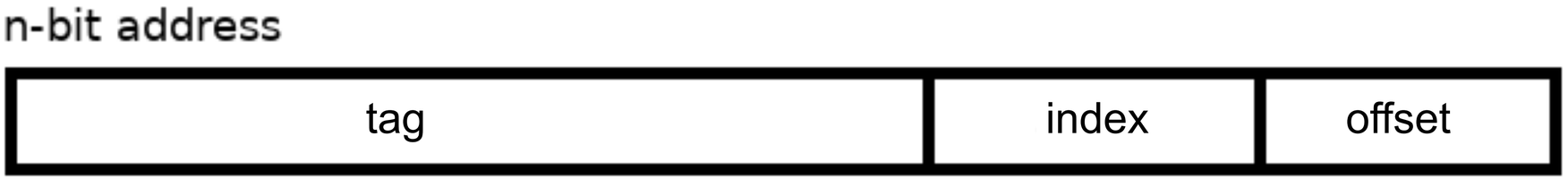
https://www.allaboutcircuits.com/technical-articles/principles-of-cache-design/

Cache structure

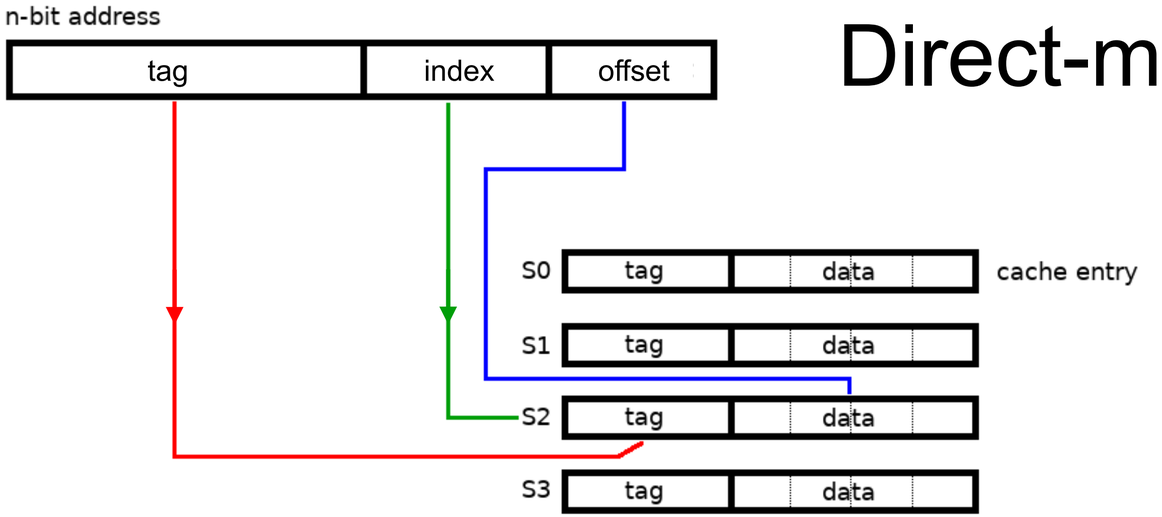
Cache entry (line)



Address (cache lookup key)



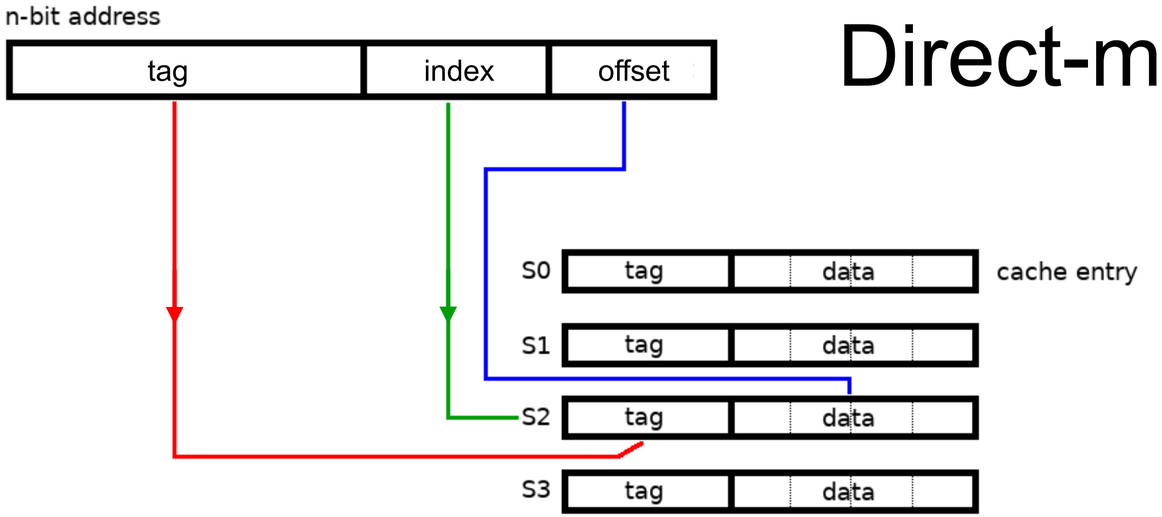
Cache structure



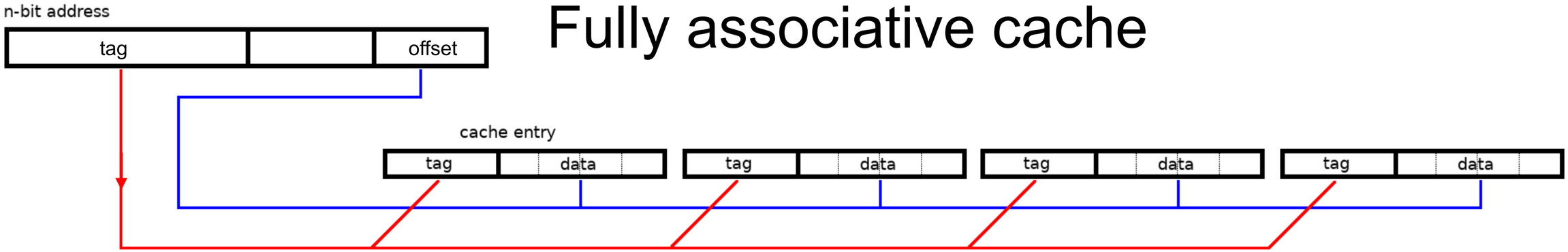
Direct-mapped cache

Cache structure

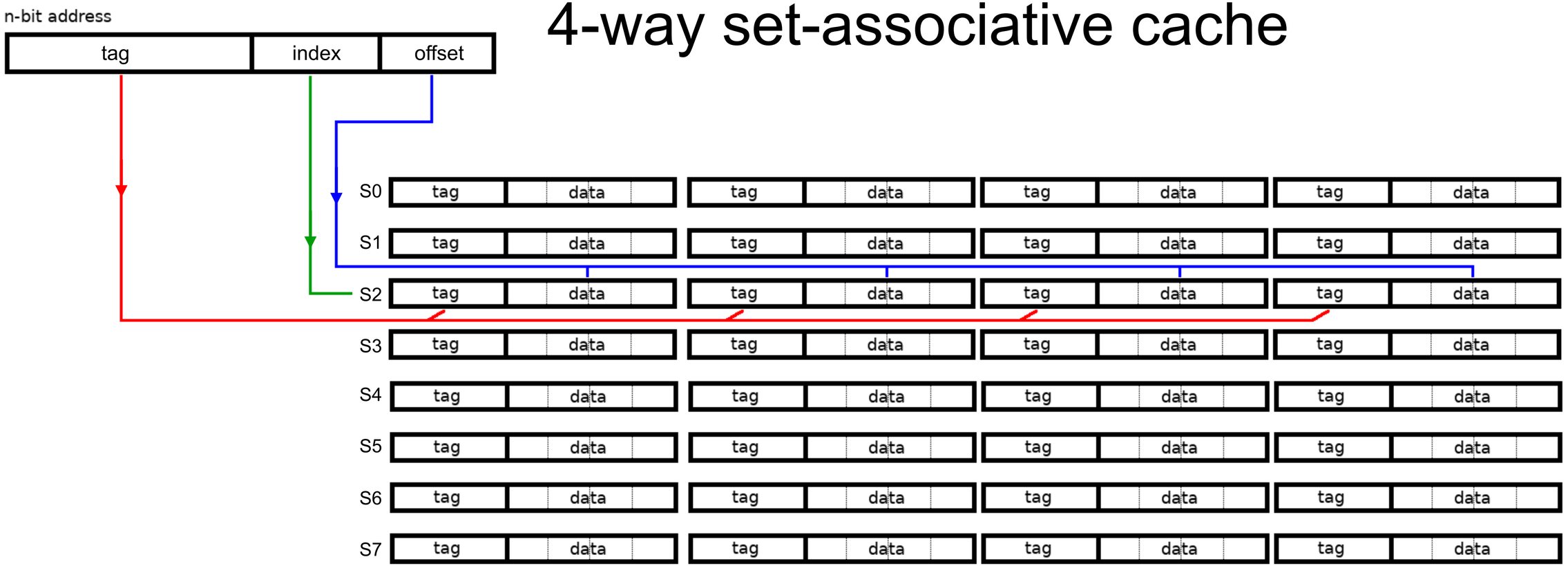
Direct-mapped cache



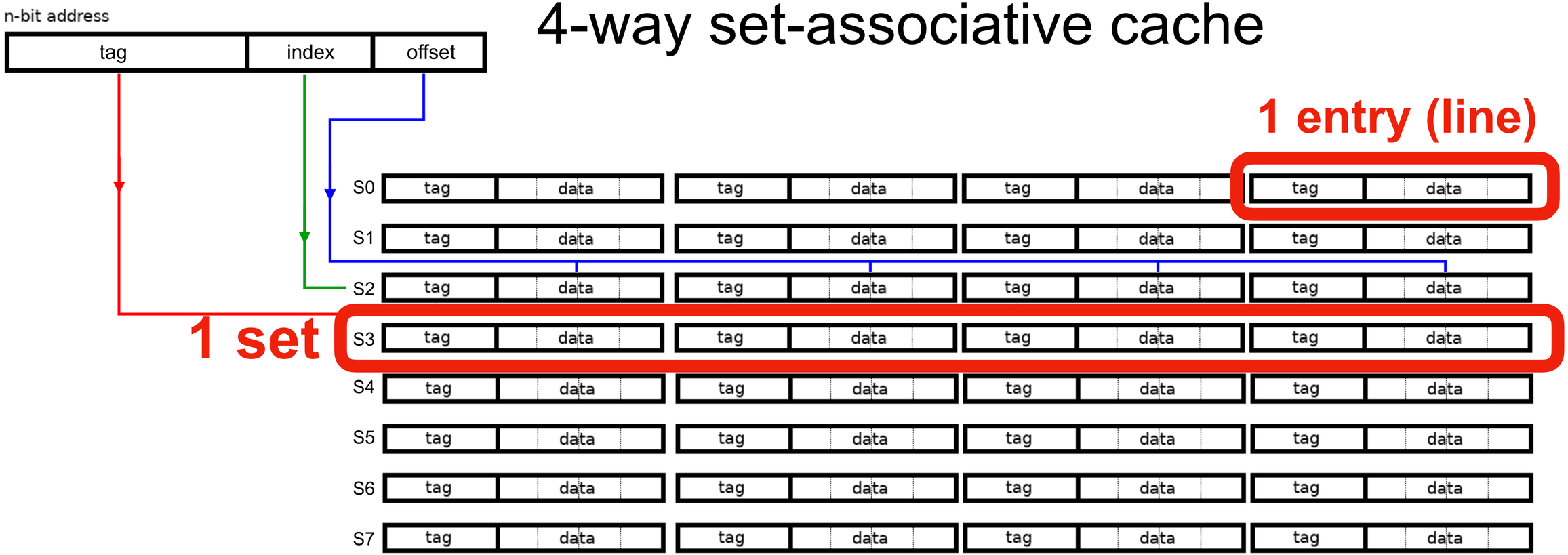
Fully associative cache



Cache structure

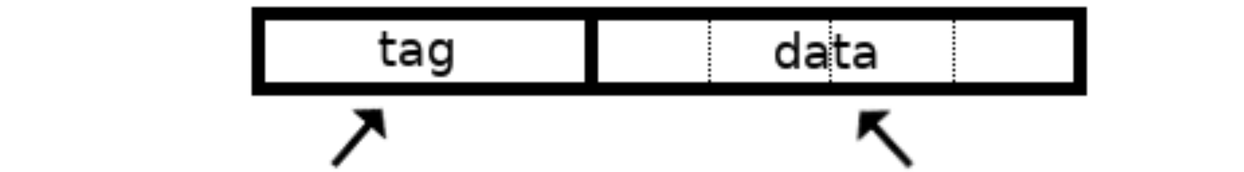


Cache structure



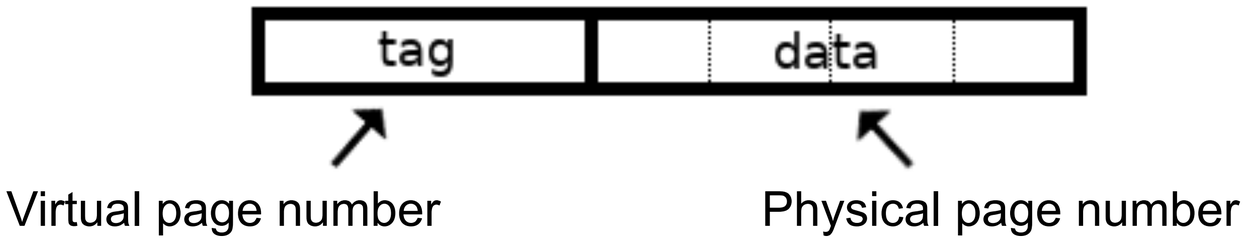
Overhead of memory-location name resolution

TLB cache line



Overhead of memory-location name resolution

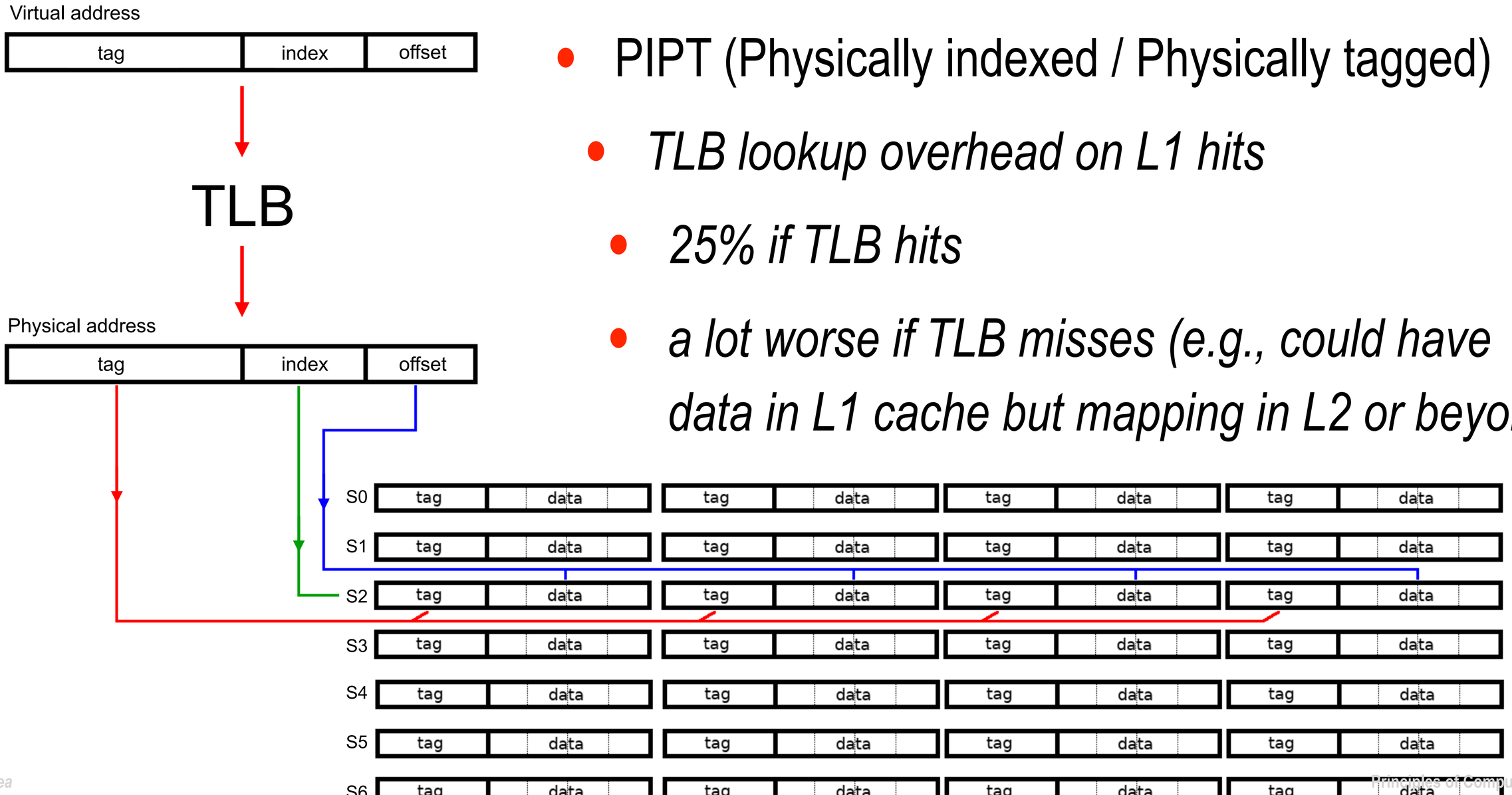
TLB cache line



- Skylake (4 KiB pages)
  - *L1 i-TLB: 16 sets * 8-way set-associative = 128 entries*
  - *L1 d-TLB: 16 sets * 4-way set associative = 64 entries*
  - *L2 shared TLB: 256 sets * 12-way set associative = 1536 entries*

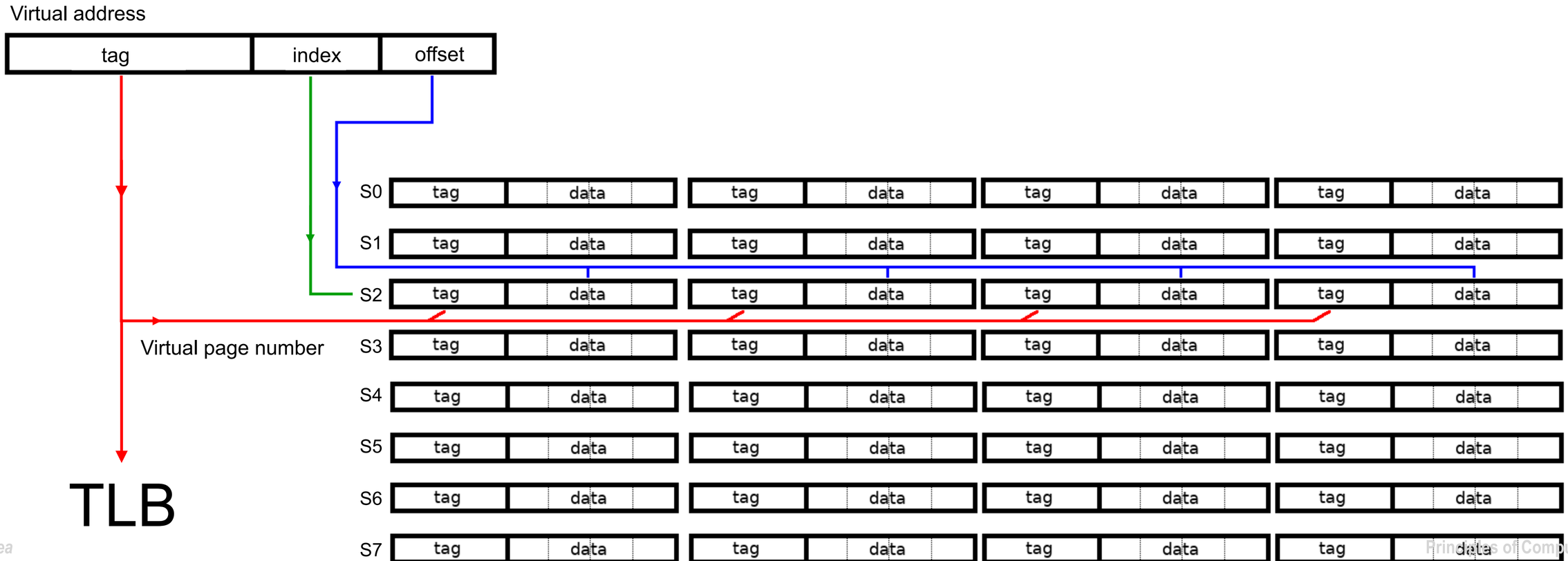
PIPT L1 d/i-cache ?

PIPT L1 d/i-cache ?



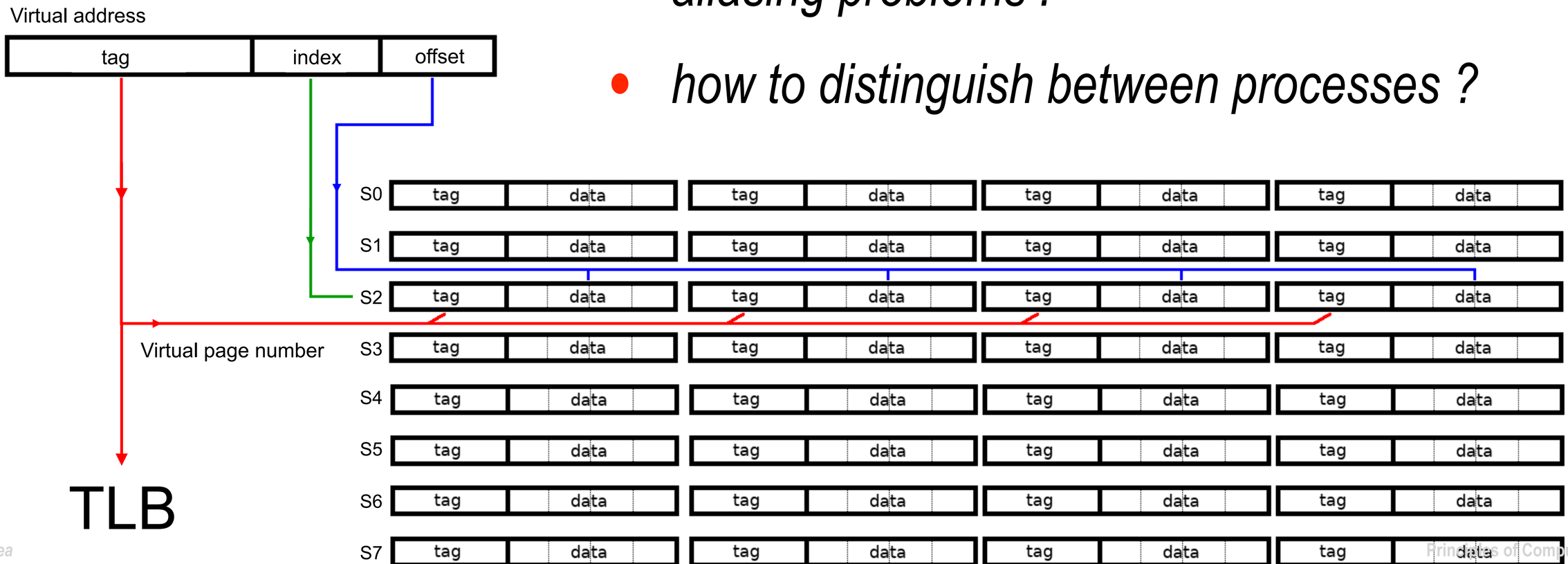
- PIPT (Physically indexed / Physically tagged)
  - *TLB lookup overhead on L1 hits*
    - *25% if TLB hits*
    - *a lot worse if TLB misses (e.g., could have data in L1 cache but mapping in L2 or beyond)*

VIVT L1 d/i-cache ?

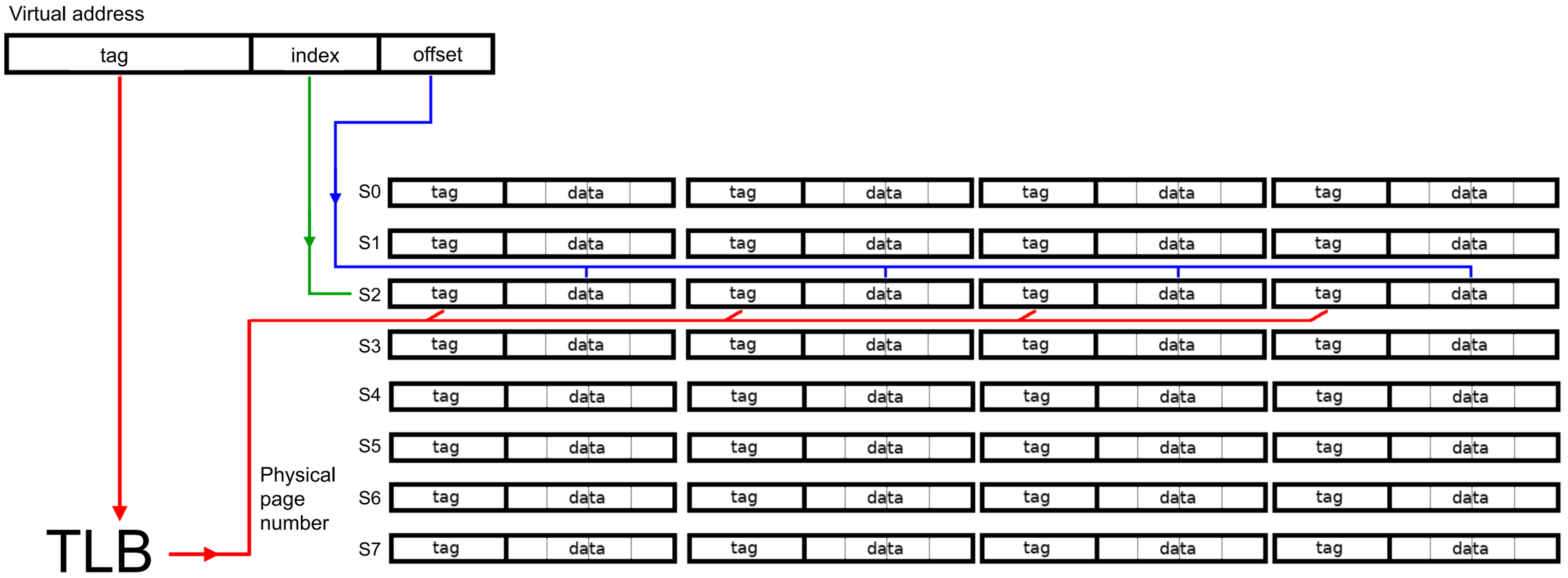


VIVT L1 d/i-cache ?

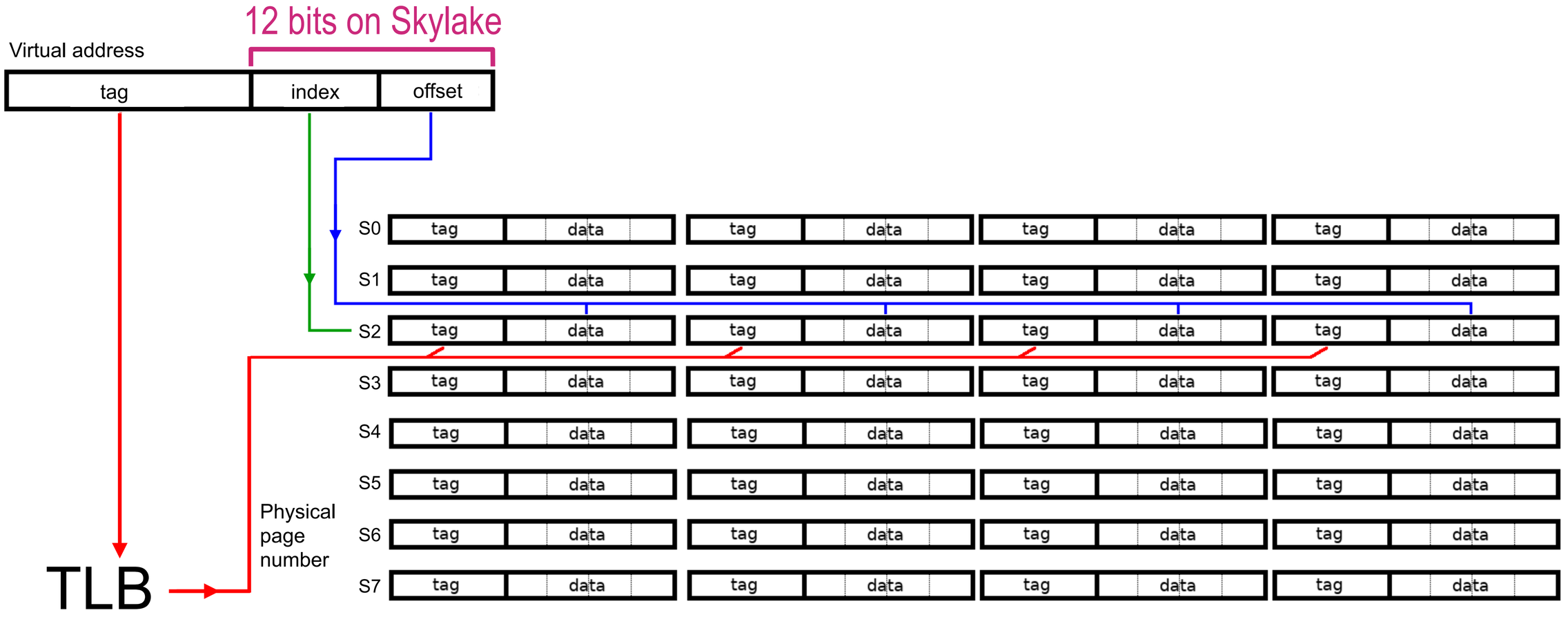
- VIVT (Virtually indexed / Virtually tagged)
  - *TLB lookups become free*
  - *aliasing problems !*
  - *how to distinguish between processes ?*



VIPT L1 d/i-cache ?

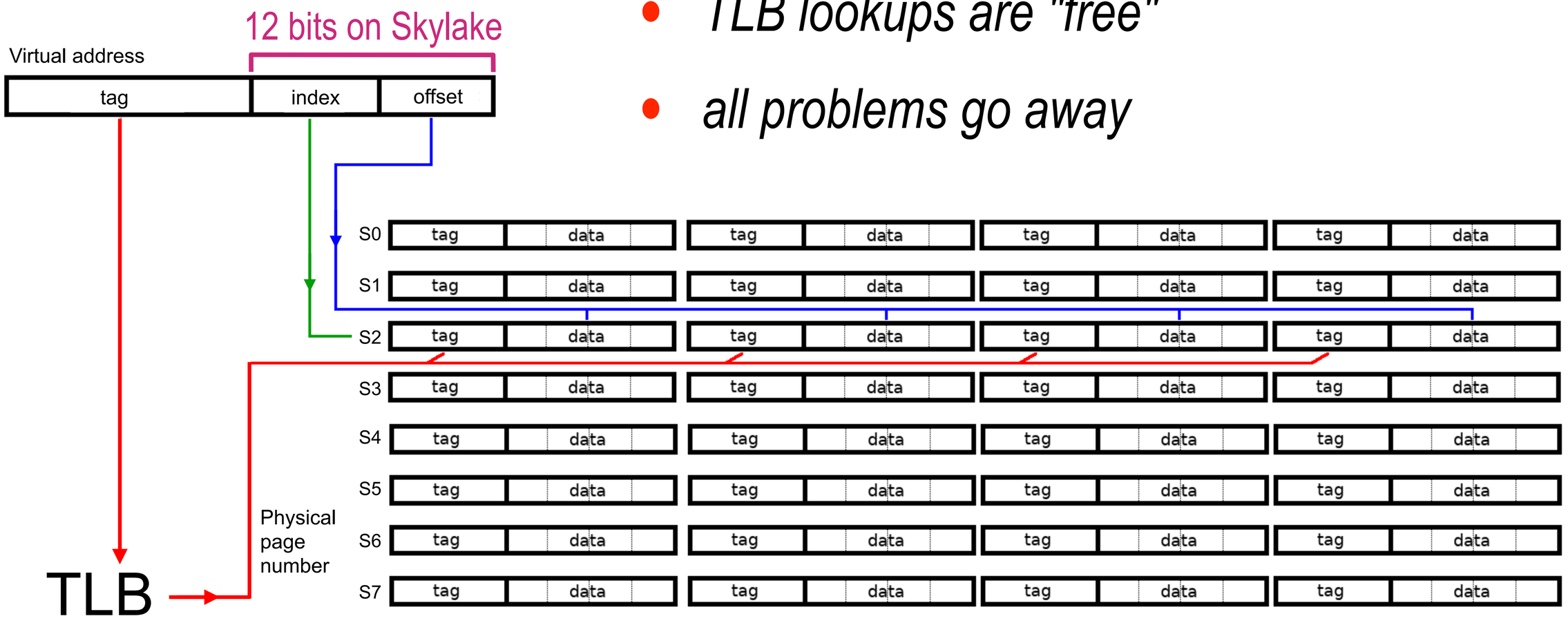


VIPT L1 d/i-cache ?



VIPT L1 d/i-cache ?

- VIPT (Virtually indexed / Physically tagged)
  - *TLB lookups are "free"*
  - *all problems go away*



Zero-cost VA-to-PA resolution

This slide is not about the TLB but about the memory cache (in particular L1, since for L2/L3 the TLB overhead is negligible)

- Types of main memory caches
  - *PIPT (Physically indexed / Physically tagged)*
    - TLB lookup introduces 25% overhead on L1 hits
  - *VIVT (Virtually indexed / Virtually tagged)*
    - Aliasing problems + how to distinguish between processes?
  - *VIPT (Virtually indexed / Physically tagged)*
    - Parallel lookup in TLB and L1 => mask entirely the TLB's (<1 cycle) as part of L1's 3-4 cycles
  - ~~*PIVT (Physically-indexed / Virtually-tagged)*~~
- Caches on x86
  - *L1 is VIPT*
  - *L2 and L3 are PIPT*

Summary

- MMU maps memory VAs (names) to PAs (values)
- Space scalability
  - *name space is sparse => use hierarchical, multi-level page tables (directories)*
  - *use pages and offsets as a way to avoid looking up every single location*
  - *reduce number name lookups by aggregating locations (huge pages)*
- Performance scalability
  - *cache mappings in TLBs*
  - *mask TLB lookup with VIPT memory caches (in the common case)*
- Make common case fast, make rare case merely correct

Reference Values for System Design

Reference Values (absolute time)

- L1 / L2 / main RAM reference ~ 1 / 4 / 40-50 ns (modern RAM like DDR4 even higher... 100+ ns)
- DRAM bandwidth ~200 GB/sec (DDR4/DDR5 multi-channel >500 GB/sec, HBM in GPUs >1 TB/sec)
- Flash SSD random access 50-100 microsec (NVMe SSDs can be even lower)
- Flash SSD bandwidth 5-15 GB/sec
- Seek on enterprise-grade HDD ~4 millisec
- Bandwidth of enterprise-grade HDD ~150 MB/sec
- Mutex lock or unlock ~ 15-100 ns *(depending on whether share cache line, are contended, are cache-aligned ...)*
- Packet RTT within a datacenter < 10 microsec (ignoring software stacks)
- Bandwidth between two hosts in a data center 10-400 Gbps
- Compress 1 KB of data (with Snappy/LZ77) ~ 2 microsec
- Packet roundtrip CA -> Amsterdam -> CA = 150 millisec (*note: speed of light in fiber ~5 msec/1,000 km)*

Reference Values (CPU cycles)

- Register-register ADD/OR/etc. < 1 CPU cycle *(in an OO, pipelined processor)*
- Register write ~1 cycle
- Correctly / incorrectly predicted "if" branch = 1 cycle / 10-20 cycles
- L1 / L2 / L3 / main RAM read = ~4 cycles / ~20 cycles / ~30-50 cycles / ~100-150 cycles
- TLB hit = 0.5 - 1 cycle (DDR4/5 250-350 cycles)
- CAS = 15-30 cycles (increases with the number of cores !)
- C function direct / indirect call = 10-20 cycles / 20-50 cycles
- Kernel crossing round-trip = 500 - 1,200 cycles
- Thread context switch (direct costs) = 2K - 15K cycles
- On NUMA, different-socket mem hierarchy access is 3 - 10x that of non-NUMA