Problem 1: Exact Synthesis

Suppose we are given a satisfying SAT assignment to an exact synthesis problem with \( n = 3 \) and \( r = 2 \). Note that this implies that the gate index \( i \) ranges from 4 to 5 and that there are 7 truth table simulation bits: from position 1 to 7.

We are given the following assignments variables \( x_i \):

\[
\begin{align*}
t &= 7 \ 6 \ 5 \ 4 \ 3 \ 2 \ 1 \\
x_{4t} &= 1 \ 0 \ 0 \ 0 \ 1 \ 0 \ 0 \\
x_{5t} &= 0 \ 1 \ 1 \ 1 \ 1 \ 0 \ 0
\end{align*}
\]

The \( g_{hi} \) variables have been assigned as follows:

\[
g_{14} = 1, \ g_{15} = 0, \ g_{24} = 0, \ g_{25} = 1
\]

The \( s_{ijk} \) variables have been assigned as follows:

\[
\begin{array}{c}
k = 2 \ 3 \ 4 \\
s_{41k} = 1 \ 0 \\
s_{42k} = 0 \\
s_{51k} = 0 \ 0 \ 0 \\
s_{52k} = 0 \ 0 \\
s_{53k} = 1
\end{array}
\]

Finally, the \( f_{ipq} \) variables have been assigned as follows:

\[
(p, q) = (1, 1) \ (0, 1) \ (1, 0) \\
f_{4pq} = 1 \ 0 \ 0 \\
f_{5pq} = 0 \ 1 \ 1
\]

Given this information, draw the corresponding logic network. What are the functions computed at the network’s outputs?
Problem 2: Timing and False Path Detection

Consider the logic network defined as:

\[ d = b'; \quad e = a \cdot d; \quad x = a + e; \]
\[ g = e \oplus c; \quad f = x'; \quad y = f \cdot g. \]

Inputs are \( \{a, b, c\} \) and outputs are \( \{x, y\} \). All logic gates have unit delay. The data ready time of all the primary inputs is 0. The data required time at the outputs is 5.

(a) Draw the logic network graph.

(b) Determine the data ready time and the slacks for all nodes.

(c) Find the topological critical paths.

(d) Are the topological critical paths statically sensitizable?

(e) Are the topological critical paths true paths? (Hint: check if they are dynamically sensitizable).