Embedded Systems

CycloneV & DE1-SoC

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FPGA WITH SOC ARCHITECTURE
2 main actors

- **Altera** (www.altera.com):
  - Cyclone V SOC
  - Arria V SOC

- **Xilinx** (www.xilinx.com):
  - Zynq® 7000 family
2 main actors, Common Features

- 2x ARM-Cortex A9 hardcore
  - 2x NEON DSP/FPU
  - Many programmable interface in hardcore
  - Amba interconnect
  - Large FPGA part
  - DDR Controller

Ex: Zynq-7000
CYCLONEV-SOC ARCHITECTURE (ALTERA)
Cyclone V SoC Overview

Altera SoC FPGA Device

HPS Portion
- Flash Controllers
- SDRAM Controller Subsystem
- Cortex-A9 MPU Subsystem
- On-Chip Memories
- Support Peripherals
- PLLs
- Interface Peripherals
- Debug

HPS-FPGA Interfaces

FPGA Portion
- Control Block
- User I/O
- HSSI Transceivers
- FPGA Fabric (LUTs, RAMs, Multipliers & Routing)
- PLLs
- Hard PCIe
- Hard Memory Controllers

Cyclone V HPS (Hard Processor System)

FPGA Portion
- FPGA Manager
- FPGA-to-HPS Bridge
- HPS-to-FPGA Bridge
- Lightweight HPS-to-FPGA Bridge
- Control Block
- Masters
- Slaves
- 32-, 64- & 128-Bit AXI
- 1 - 6 Masters

System Manager
- L4, 32-Bit Bus
- DAP
- ETR
- SD/MMC
- EMAC
- USB OTG
- NAND Flash
- L3 Interconnect (NIC-301)
- L3 Master Peripheral Switch
- L3 Slave Peripheral Switch
- 32-Bit
- 64-Bit AXI
- 32-Bit AXI

MPU Subsystem
- ARM Cortex-A9 MPICore
- CPU0
- CPU1
- ACP ID Mapper
- ACP
- SCU
- L2 Cache
- STM
- Boot ROM
- On-Chip RAM
- DMA
- SDRAM Controller Subsystem
- Quad SPI Flash

I/O part
- L4, 32-Bit Bus
- CAN
- Timer
- I²C
- Watchdog Timer
- UART
- GPIO
- SPI
- Clock Manager
- Reset Manager
- Scan Manager
- System Manager

A2015
HPS-FPGA Address Space

- Peripheral Region
  - FPGA Slaves Region
  - ACP Window
  - SDRAM Window
  - RAM / SDRAM
  - L3

- Lightweight FPGA Slaves Region
  - SDRAM Window
  - Boot Region (ROM/RAM/SDRAM)

- MPU

- SDRAM Region
  - 4 GB
  - 3 GB
  - 2 GB
  - 1 GB
  - 0 GB

A2015
Clock manager
Abbreviation

- STM  System Trace Module
- DMA  Direct Memory Access
- DAP  Debug Access Port
- ETR  Embedded Trace Router
- SD/  Support: SDSC(SD), SDHC, SDXC, eSD, SDIO, eSDIO
- MMC  MMC, RSMMC, MMCPlus, MMCMobile, eMMC
- EMAC Ethernet Media Access Controller
Abbreviation

- ACP  Accelerator Coherency Port
- USB
- UART
- SPI
- CAN
- I2C
Ex. Programmable Interface SD/MMC Unit
Boot process

• It is possible to use the Cyclone V SoC in 3 different configurations:
  - FPGA-only
  - HPS-only
  - HPS & FPGA

• The configurations using the HPS are more difficult to set up than the *FPGA-only* one.
HPS/FPGA Boot (1) Independent FPGA Configuration and HPS Booting
HPS/FPGA Boot (2)  FPGA Configuration before HPS Booting (HPS boots from FPGA)

FPGA Portion

- Active Serial/Active Serial x4
- Passive Serial
- Passive Parallel

FPGA Fabric

HPS Portion

- MPU
- HPS-to-FPGA Bridge
- Boot ROM

Altera SoC Device

Boot & Configuration Sources

PCle
HPS/FPGA Boot (3) - HPS Boots and Performs FPGA Configuration

Altera SoC Device

FPGA Portion

HPS Portion

FPGA Fabric

MPU

Quad SPI Flash Controller

SD/MMC Flash Controller

NAND Flash Controller

EMAC

Boot Sources

Configuration Source
FPGA only case

• Exclusively using the FPGA part of the Cyclone V is easy, as the design process is identical to any other Altera FPGA.

• We can build a complete design in Quartus II & Qsys, simulate it in ModelSim-Altera, then program the FPGA through the Quartus II Programmer.

• We can instantiate a Nios II processor in Qsys, we can use the Nios II SBT IDE to develop software for the processor.
Type of Application

• OS based (ie: Linux)
• Bare-metal (No OS)
Although the HPS has a **DUAL**-processor, CPU1 is under reset, and the boot flow only executes on CPU0.

If we want to use both processors, then **USER SOFTWARE** executing on CPU0 is responsible for releasing CPU1 from reset.
Preloader

• The preloader is one of the most important boot stages. It is actually what one would call the boot “source”, as all stages before it are unmodifiable. The preloader can be stored on external flash-based memory, or in the FPGA fabric.

• The preloader typically performs the following actions:
  - Initialize the SDRAM interface
  - Configure the HPS I/O through the scan manager
  - Configure pin multiplexing through the system manager
  - Configure HPS clocks through the clock manager
  - Initialize the flash controller (NAND, SD/MMC, QSPI) that contains the next stage boot software
  - Load the next boot software into the SDRAM and pass control to it

• The preloader does NOT release CPU1 from reset. The subsequent stages of the boot process are responsible for it if they want to use the extra processor.
Project structure
DE1-SOC Bloc Diagramm
Green for peripherals directly connected to the FPGA
Orange for peripherals directly connected to the HPS
Blue for board control
Qsys, hps definition (1)
IO PIN in HPS

• With the *PeripheralPin Multiplexing*, some I/O interface can be used by the **HPS part** or the **FPGA part**.
• The selection is done here.
Exercises / Mini Project

1. Use the DE1-SOC without the ARM-A9
   - NIOS design to access the Switches and LEDs
   - Adapt the LCD/camera controller for the NIOSII

2. Use the ARM-A9 with ARM DS-5 software
   - Access through the AXI bridge the Avalon part of the FPGA
   - Control the LCD/camera from the ARM
• Try the Linux access of the FPGA…to control LCD and Camera

• In option!