TFT-LCD Display + Camera

Design of a TFT Controller & Camera Controller For FPGA

Avalon Master/Slave device

rene.beuchat@epfl.ch
rene.beuchat@hesge.ch
Goals

• The goal is to understand how to design a master unit for a System on FPGA
• 2 masters units have to be designed:
  ➢ a LCD controller
  ➢ a camera controller
• A system with a NIOSII on FPGA has to be build
• A software to control the display and the camera acquisition
Camera (TRDB-D5M) & LCD (LT24)

With DE1-SOC

With DE0-nano
Video Controllers in FPGA, General architecture

- Camera Module
- Camera Ctrl
- NIOSII
- SRAM
- LCD Ctrl
- Avalon Bus
- Master
- Slave
- M/S
- FPGA
- SDRAM
- JTAG
- LCD Ctrl
- Display LCD
- Memory SDRAM

R看望
LCD (LT24) specifications

• In this example, the LT24 module from terasic is used (www.terasic.com), characteristics:
  ➢ 240 (H) x 320 (V) RGB 5-6-5 bits/color
  ➢ Touch Panel, resistive technology
  ➢ Small LCD extension on 40 pins connector
  ➢ Simple access to the module as a programmable interface
  ➢ Main controller ILI9341 (Ilitek)
LT24 for DE0-nano & DE1-SOC

• Interface signals:
  ➢ LCD_ON
  ➢ Reset_n
  ➢ CS_n
  ➢ RS (reg. Sel. C/nD)
  ➢ Wr_n
  ➢ Rd_n
  ➢ D[15..0]

[Diagram of interface signals and connections]
2x20 pins connection

DE0-nano

VCC_SYS

GPIO_0_IN0 1
GPIO_0 IN1 3
GPIO_02 5
GPIO_04 7
GPIO_06 9
GPIO_08 11
GPIO_10 13
GPIO_012 15
GPIO_014 17
GPIO_016 19
GPIO_018 21
GPIO_020 23
GPIO_022 25
GPIO_024 27
GPIO_026 29
GPIO_028 31
GPIO_030 33
GPIO_032 35
GPIO_034 37
GPIO_036 39
GPIO_00 2
GPIO_01 4
GPIO_03 6
GPIO_05 8
GPIO_07 10
GPIO_09 12
GPIO_011 14
GPIO_013 16
GPIO_015 18
GPIO_017 20
GPIO_019 22
GPIO_021 24
GPIO_023 26
GPIO_025 28
GPIO_027 30
GPIO_029 32
GPIO_031 34
GPIO_033 36

VCC3P3

LT24

ADC_PENIRO_n
ADC_BUSY
ADC_DCLK
DB0
DB2
DB0
ADC_DOUT
ADC_DOUT

VCC5

RD_n
RS
DB5
DB7
DB9
DB11
DB13
DB15

VCC3.3

ADC_CS_n
RESET_n
LCD_ON

Female Header 2x20 GPIO
FPGA - LT24 ILI9441 connection

- 65'536 colors 5-6-5 RGB
- 8080-system I, 16 bits interface
- Ref: §7.6.5 ILITEK ILI9341
LT24: Bus interface

- CSx: CS_n Chip Select
- D/Cx: D/Cn Data / Command_n
- WRx: WR_n Write Access
- RDx: RD_n Read Access
LT24 Timing Diagram Connection, Write Command/Data

<table>
<thead>
<tr>
<th>IM3</th>
<th>IM2</th>
<th>IM1</th>
<th>IM0</th>
<th>MCU-Interface Mode</th>
<th>GSX</th>
<th>WRX</th>
<th>RDX</th>
<th>D/CX</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>8080 MCU 16-bit bus interface I</td>
<td>“L”</td>
<td>“H”</td>
<td>“L”</td>
<td>“H”</td>
<td>Write command code.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>“L”</td>
<td>“H”</td>
<td>“L”</td>
<td>“H”</td>
<td>Read internal status.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>“L”</td>
<td>“H”</td>
<td>“H”</td>
<td>“H”</td>
<td>Write parameter or display data.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>“L”</td>
<td>“H”</td>
<td>“H”</td>
<td>“H”</td>
<td>Reads parameter or display data.</td>
</tr>
</tbody>
</table>

---

**Interface**

- CSX
- RESX
- D/CX
- WRX
- RDX

**D[17:0]**

- Command Address
- Command Data

**D[17:0] (LCD to Host)**

- Hi-Z

**D[17:0] Host to LCD**

---

RB 2006/A2015
LT24 Timing Diagram Connection, Read Command/Data

- Write Command, Read Dummy, Read Data

![LT24 Timing Diagram](image)
LT24 Timing Access

• The interface used is the old fashion 8080-system 16 bits wide.
• The transfers are asynchronous (no clock related) between the FPGA and the module
• The data are sent line by line by burst of 240 pixels continuously
LCD data transfers format, 16 bits data mode

For each line of LCD:
5 bits Blue, 6 bits Green, 5 bits Red, \( IM[3:0]: \text{“0001”} \)

Register 3Ah: \( \text{“xxxxxx101”}, \ MDT[1..0]: \text{“00”} \)

<table>
<thead>
<tr>
<th>Count</th>
<th>0</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>...</th>
<th>238</th>
<th>239</th>
<th>240</th>
</tr>
</thead>
<tbody>
<tr>
<td>D/CX</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>...</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>D15</td>
<td>0R4</td>
<td>1R4</td>
<td>2R4</td>
<td>...</td>
<td>237R4</td>
<td>238R4</td>
<td>239R4</td>
<td></td>
</tr>
<tr>
<td>D14</td>
<td>0R3</td>
<td>1R3</td>
<td>2R3</td>
<td>...</td>
<td>237R3</td>
<td>238R3</td>
<td>239R3</td>
<td></td>
</tr>
<tr>
<td>D13</td>
<td>0R2</td>
<td>1R2</td>
<td>2R2</td>
<td>...</td>
<td>237R2</td>
<td>238R2</td>
<td>239R2</td>
<td></td>
</tr>
<tr>
<td>D12</td>
<td>0R1</td>
<td>1R1</td>
<td>2R1</td>
<td>...</td>
<td>237R1</td>
<td>238R1</td>
<td>239R1</td>
<td></td>
</tr>
<tr>
<td>D11</td>
<td>0R0</td>
<td>1R0</td>
<td>2R0</td>
<td>...</td>
<td>237R0</td>
<td>238R0</td>
<td>239R0</td>
<td></td>
</tr>
<tr>
<td>D10</td>
<td>0G5</td>
<td>1G5</td>
<td>2G5</td>
<td>...</td>
<td>237G5</td>
<td>238G5</td>
<td>239G5</td>
<td></td>
</tr>
<tr>
<td>D9</td>
<td>0G4</td>
<td>1G4</td>
<td>2G4</td>
<td>...</td>
<td>237G4</td>
<td>238G4</td>
<td>239G4</td>
<td></td>
</tr>
<tr>
<td>D8</td>
<td>0G3</td>
<td>1G3</td>
<td>2G3</td>
<td>...</td>
<td>237G3</td>
<td>238G3</td>
<td>239G3</td>
<td></td>
</tr>
<tr>
<td>D7</td>
<td>C7</td>
<td>C7</td>
<td>C7</td>
<td>C7</td>
<td>...</td>
<td>237G1</td>
<td>238G1</td>
<td>239G1</td>
</tr>
<tr>
<td>D6</td>
<td>C6</td>
<td>C6</td>
<td>C6</td>
<td>C6</td>
<td>...</td>
<td>237G0</td>
<td>238G0</td>
<td>239G0</td>
</tr>
<tr>
<td>D5</td>
<td>C5</td>
<td>C5</td>
<td>C5</td>
<td>C5</td>
<td>...</td>
<td>237B4</td>
<td>238B4</td>
<td>239B4</td>
</tr>
<tr>
<td>D4</td>
<td>C4</td>
<td>C4</td>
<td>C4</td>
<td>C4</td>
<td>...</td>
<td>237B3</td>
<td>238B3</td>
<td>239B3</td>
</tr>
<tr>
<td>D3</td>
<td>C3</td>
<td>C3</td>
<td>C3</td>
<td>C3</td>
<td>...</td>
<td>237B2</td>
<td>238B2</td>
<td>239B2</td>
</tr>
<tr>
<td>D2</td>
<td>C2</td>
<td>C2</td>
<td>C2</td>
<td>C2</td>
<td>...</td>
<td>237B1</td>
<td>238B1</td>
<td>239B1</td>
</tr>
<tr>
<td>D1</td>
<td>C1</td>
<td>C1</td>
<td>C1</td>
<td>C1</td>
<td>...</td>
<td>237B0</td>
<td>238B0</td>
<td>239B0</td>
</tr>
<tr>
<td>D0</td>
<td>C0</td>
<td>C0</td>
<td>C0</td>
<td>C0</td>
<td>...</td>
<td>237B0</td>
<td>238B0</td>
<td>239B0</td>
</tr>
</tbody>
</table>
LCD Controller in FPGA

• To control the LCD, a Controller is necessary

• For FPGA4U and in a system based on a NIOSII processor on **Avalon Bus** a specific interface is to be designed.

• It needs to be an:
  - Avalon slave to program it
  - Avalon Master to take display information in memory
LCD Controller in FPGA, General architecture

- Display
- LCD
- Slave
- Master
- M/S
- LCD Ctrl
- NIOSII
- SDRAM Ctrl
- Avalon Bus
- FPGA
- JTAG
- Epcs ctrl
- Memory
- EP16
- Addresses
- Control
- Data

EPFL

RB 2006/A2015
To configure the LCD controller, a number of registers needs to be defined and implemented.

They need to be programmed by the processor at startup.

They have default values.

A command register start the controller and control the power converter and LCD enable.
## Reset Initialization §15.1 p.228

<table>
<thead>
<tr>
<th></th>
<th>After Powered ON</th>
<th>After Hardware Reset</th>
<th>After Software Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frame Memory</td>
<td>Random</td>
<td>Repair data</td>
<td>No Change</td>
</tr>
<tr>
<td>Sleep</td>
<td>In</td>
<td>In</td>
<td>In</td>
</tr>
<tr>
<td>Display Mode</td>
<td>Normal</td>
<td>Normal</td>
<td>Normal</td>
</tr>
<tr>
<td>Display</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Idle</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>Column Start Address</td>
<td>0000 h</td>
<td>0000 h</td>
<td>0000 h</td>
</tr>
<tr>
<td>Column End Address</td>
<td>00EF h</td>
<td>00EF h</td>
<td>If MADCTL’s B5 = 0:00EF h</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If MADCTL’s B5 = 1:013F h</td>
</tr>
<tr>
<td>Page Start Address</td>
<td>00000 h</td>
<td>00000 h</td>
<td>0000 h</td>
</tr>
<tr>
<td>Page End Address</td>
<td>013F h</td>
<td>013F h</td>
<td>If MADCTL’s B5 = 0:013F h</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If MADCTL’s B5 = 1:00EF h</td>
</tr>
<tr>
<td>Gamma Setting</td>
<td>GC0</td>
<td>GC0</td>
<td>GC0</td>
</tr>
<tr>
<td>Partial Area Start</td>
<td>0000 h</td>
<td>0000 h</td>
<td>0000 h</td>
</tr>
<tr>
<td>Partial Area End</td>
<td>013F h</td>
<td>013F h</td>
<td>013F h</td>
</tr>
<tr>
<td>Memory Data Access</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Control</td>
<td>00 h</td>
<td>00 h</td>
<td>No Change</td>
</tr>
<tr>
<td>RDDPM</td>
<td>08 h</td>
<td>08 h</td>
<td>08 h</td>
</tr>
<tr>
<td>RDDDMADCTL</td>
<td>00 h</td>
<td>00 h</td>
<td>No Change</td>
</tr>
<tr>
<td>RDDCOLMOD</td>
<td>06 h</td>
<td>06 h</td>
<td>06 h</td>
</tr>
<tr>
<td>RDDIM</td>
<td>00 h</td>
<td>00 h</td>
<td>00 h</td>
</tr>
<tr>
<td>RDDSM</td>
<td>00 h</td>
<td>00 h</td>
<td>00 h</td>
</tr>
<tr>
<td>RDDSDR</td>
<td>00 h</td>
<td>00 h</td>
<td>00 h</td>
</tr>
<tr>
<td>TE Output Line</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>TE Line Mode</td>
<td>Mode 1 (Note 3)</td>
<td>Mode 1 (Note 3)</td>
<td>Mode 1 (Note 3)</td>
</tr>
</tbody>
</table>
Detailed timing diagram

<table>
<thead>
<tr>
<th>WRX</th>
<th>twc</th>
<th>Write cycle</th>
<th>66</th>
<th>-</th>
<th>ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>twrh</td>
<td></td>
<td>Write Control pulse H duration</td>
<td>15</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>twrl</td>
<td></td>
<td>Write Control pulse L duration</td>
<td>15</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>
LCD Controller architecture
LCD Control architecture

- The LCD Controller can be separate in 4 main blocks:
  - **Avalon Slave** to access registers
  - **Avalon Master** to read memory
  - A **FIFO** to receive data from Avalon Master and provide them to LCD control part
    The FIFO guarantees a *continuous* flow from memory the LCD, as memory is shared by multiples masters
  - A **LCD Control** to sequence the LCD signals and send RGB data
The Avalon slave interface is used to:

- receive and send registers contents from/to a Master Processor (ie: the NIOSII)
- Send an IRQ at end of frame if enabled, this allows the processor to provide a new buffer address at start of display frame
- Dispatch the registers content to the modules:
  - Buffer information to master interface
  - Display parameters to LCD Control
The Avalon Master interface is used to:

1. Receive the Buffer information from Avalon slave part as:
   - Start address of the buffer
   - Length of buffer to read
2. Synchronize the start of reading with LCD VSync from LCD Ctrl
3. Read display data from memory through Avalon read accesses
4. Send the Read data to a synchronization FIFO
Address and BurstCount available for the first cycle only
Read signal only for the first cycle
The number of burstcount ReadDataValid needs to be generated
The master could start a new transfer in 2
Interface Camera, FIFO

- A FIFO (First In First Out) Memory allows the synchronization between a data producer and a data reader with asynchronous transfers rate.
- Available and configurable with QuartusII MegaWizard

![FIFO Diagram]

- FIFO_Empty
- FIFO_Almost_Empty
- RdFIFO
- Clk
- FIFO_Full
- FIFO_Almost_Full
- WrFIFO
- Clk
- RdData
- WrData
FIFO

• The Output `FIFO_Alpmost_Empty` allows to know if they are still `xx` free positions in the FIFO and `FIFO_Alpmost_Full` allows to know if they are already `xx` filled positions in the FIFO

• `xx` programmable when FIFO is generated with MegaWizard

• Thus it is possible to know that at least Burst Mode Size data are available for read access master transfers to write in FIFO

• The size off the FIFO and …_Almost_... are defined at generation time of the FIFO through MegaWizard
Some ILI9341 Commands
<table>
<thead>
<tr>
<th>Command Function</th>
<th>D/CX</th>
<th>RXD</th>
<th>WRX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>Hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Operation</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>00h</td>
</tr>
<tr>
<td>Software Reset</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>01h</td>
<td></td>
</tr>
<tr>
<td>Read Display Identification Information</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>04h</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>ID1 [7:0]</td>
<td></td>
<td>XX</td>
<td>07h</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>ID2 [7:0]</td>
<td></td>
<td>XX</td>
<td>07h</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>ID3 [7:0]</td>
<td></td>
<td>XX</td>
<td>07h</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read Display Status</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>D [31:25]</td>
<td>X</td>
<td>00</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>D [22:20]</td>
<td></td>
<td>X</td>
<td>D [19:16]</td>
<td>61</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>D [18:12]</td>
<td></td>
<td>X</td>
<td>X</td>
<td>D [10:8]</td>
<td>00</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Read Display Power Mode</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>06h</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>D [7:5]</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Read Display MADCTL</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>06h</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>D [7:2]</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Read Display Pixel Format</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>06h</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>D [6:0]</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Read Display Image Format</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>06h</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>D [2:0]</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Read Display Signal Mode</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>06h</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>D [7:2]</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Read Display Self-Diagnostic Result</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>06h</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>D [7:2]</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Enter Sleep Mode</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>10h</td>
</tr>
<tr>
<td>Sleep OUT</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>11h</td>
</tr>
<tr>
<td>Partial Mode ON</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>12h</td>
</tr>
<tr>
<td>Normal Display Mode ON</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>13h</td>
</tr>
<tr>
<td>Display Inversion OFF</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>20h</td>
</tr>
<tr>
<td>Display Inversion ON</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>21h</td>
</tr>
<tr>
<td>Gamma Set</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>26h</td>
</tr>
<tr>
<td>Display OFF</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>28h</td>
</tr>
<tr>
<td>Display ON</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>29h</td>
</tr>
<tr>
<td>Column Address Set</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>2Ah</td>
</tr>
<tr>
<td>Page Address Set</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>28h</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>SC [15:8]</td>
<td></td>
<td>XX</td>
<td>08h</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>SC [7:0]</td>
<td></td>
<td>XX</td>
<td>08h</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>EC [15:8]</td>
<td></td>
<td>XX</td>
<td>08h</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>EC [7:0]</td>
<td></td>
<td>XX</td>
<td>08h</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>28h</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>SP [15:8]</td>
<td></td>
<td>XX</td>
<td>09h</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>SP [7:0]</td>
<td></td>
<td>XX</td>
<td>09h</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>EP [15:8]</td>
<td></td>
<td>XX</td>
<td>09h</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td></td>
<td>EP [7:0]</td>
<td></td>
<td>XX</td>
<td>09h</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Function</td>
<td>Byte 1</td>
<td>Byte 2</td>
<td>Byte 3</td>
<td>Byte 4</td>
<td>Byte 5</td>
<td>Byte 6</td>
<td>Byte 7</td>
<td>Byte 8</td>
<td>Byte 9</td>
<td>Byte 10</td>
<td>Byte 11</td>
<td>Byte 12</td>
<td>Byte 13</td>
</tr>
<tr>
<td>----------------------------------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
</tr>
<tr>
<td>Command Function</td>
<td>Command</td>
<td>CRUX</td>
<td>WRX</td>
<td>D17-8</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>Hex</td>
</tr>
<tr>
<td>----------------------------------</td>
<td>---------</td>
<td>------</td>
<td>------</td>
<td>-------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>------</td>
</tr>
<tr>
<td>RGB Interface Signal Control</td>
<td></td>
<td>0, 1</td>
<td></td>
<td>XX</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Frame Control (In Normal Mode)</td>
<td>0, 1</td>
<td>1, 1</td>
<td></td>
<td>XX</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Frame Control (In Idle Mode)</td>
<td>0, 1</td>
<td>1, 1</td>
<td></td>
<td>XX</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Frame Control (In Partial Mode)</td>
<td>0, 1</td>
<td>1, 1</td>
<td></td>
<td>XX</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Display Inversion Control</td>
<td>0, 1</td>
<td>1, 1</td>
<td></td>
<td>XX</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Blanking Porch Control</td>
<td>0, 1</td>
<td>1, 1</td>
<td></td>
<td>XX</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Extended Command Set</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Extended Command Set:

<table>
<thead>
<tr>
<th>Command Function</th>
<th>D/CX</th>
<th>RDX</th>
<th>WRX</th>
<th>D17-8</th>
<th>D7</th>
<th>D6</th>
<th>D5</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>Hex</th>
</tr>
</thead>
<tbody>
<tr>
<td>RGB Interface Signal Control</td>
<td>0, 1</td>
<td>1</td>
<td></td>
<td>XX</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>B0h</td>
</tr>
<tr>
<td>Frame Control (In Normal Mode)</td>
<td>0, 1</td>
<td>1</td>
<td></td>
<td>XX</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>B1h</td>
</tr>
<tr>
<td>Frame Control (In Idle Mode)</td>
<td>0, 1</td>
<td>1</td>
<td></td>
<td>XX</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>B2h</td>
</tr>
<tr>
<td>Frame Control (In Partial Mode)</td>
<td>0, 1</td>
<td>1</td>
<td></td>
<td>XX</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>B3h</td>
</tr>
<tr>
<td>Display Inversion Control</td>
<td>0, 1</td>
<td>1</td>
<td></td>
<td>XX</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>B4h</td>
</tr>
<tr>
<td>Blanking Porch Control</td>
<td>0, 1</td>
<td>1</td>
<td></td>
<td>XX</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>B5h</td>
</tr>
<tr>
<td>Function</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>6</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>A</td>
<td>B</td>
<td>C</td>
</tr>
<tr>
<td>--------------------------</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>Display Function Control</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Entry Mode Set</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Backlight Control 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Backlight Control 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Backlight Control 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Backlight Control 4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Backlight Control 5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Backlight Control 7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCOM Control 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCOM Control 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NV Memory Write</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NV Memory Protection Key</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NV Memory Status Read</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Read ID4

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>1</th>
<th>XX</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>D3ff</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>XX</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

### Positive Gamma Correction

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>1</th>
<th>XX</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>E0h</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VP0 [3:0]</td>
<td>08</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>VP1 [5:0]</td>
<td>0E</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>VP2 [5:0]</td>
<td>12</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VP4 [3:0]</td>
<td>05</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VP5 [4:0]</td>
<td>03</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VP6 [3:0]</td>
<td>09</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>VP20 [6:0]</td>
<td>47</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>VP36 [3:0]</td>
<td>VP27 [3:0]</td>
<td>86</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>VP43 [6:0]</td>
<td>2B</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VP50 [3:0]</td>
<td>05</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VP57 [4:0]</td>
<td>04</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VP59 [3:0]</td>
<td>00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VP61 [5:0]</td>
<td>00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VP62 [5:0]</td>
<td>00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VP63 [3:0]</td>
<td>00</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>E1h</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VN0 [3:0]</td>
<td>08</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>VN1 [5:0]</td>
<td>1A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>VN2 [5:0]</td>
<td>20</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>VN4 [3:0]</td>
<td>07</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VN5 [4:0]</td>
<td>0E</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VN6 [3:0]</td>
<td>05</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VN20 [6:0]</td>
<td>3A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>VN36 [3:0]</td>
<td>VN27 [3:0]</td>
<td>8A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VN43 [6:0]</td>
<td>40</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VN50 [3:0]</td>
<td>04</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VN57 [4:0]</td>
<td>18</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VN59 [3:0]</td>
<td>0F</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VN61 [5:0]</td>
<td>3F</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>VN62 [5:0]</td>
<td>3F</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Negative Gamma Correction

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>1</th>
<th>XX</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>E2h</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>RGA0 [3:0]</td>
<td>BCA0 [3:0]</td>
<td>XX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>RCAF [3:0]</td>
<td>BCAF [3:0]</td>
<td>XX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Digital Gamma Control 1

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>1</th>
<th>XX</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>E3h</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>RCAF [3:0]</td>
<td>BCAF [3:0]</td>
<td>XX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>RCAF [3:0]</td>
<td>BCAF [3:0]</td>
<td>XX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Digital Gamma Control 2

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>1</th>
<th>XX</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>0</th>
<th>E8h</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>RFA0 [3:0]</td>
<td>BFA0 [3:0]</td>
<td>XX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>RFA0 [3:0]</td>
<td>BFA0 [3:0]</td>
<td>XX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 1st Parameter

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>1</th>
<th>XX</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>E9h</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>MY FOR</td>
<td>MIX FOR</td>
<td>MV FOR</td>
<td>VS FOR</td>
<td>X</td>
<td>X</td>
<td>WMD</td>
<td>01</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>EPF [1:0]</td>
<td>X</td>
<td>X</td>
<td>MDT [1:0]</td>
<td>00</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Interface Control

<table>
<thead>
<tr>
<th>0</th>
<th>1</th>
<th>1</th>
<th>XX</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>F6h</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>XX</td>
<td>X</td>
<td>X</td>
<td>ENDIAN</td>
<td>X</td>
<td>X</td>
<td>DM [1:0]</td>
<td>00</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
void LCD_Init()
{
    alt_u16 data1, data2;
    alt_u16 data3, data4;
    Set_LCD_RST;
    Delay_Ms(1);
    Clr_LCD_RST;
    Delay_Ms(10);  // Delay 10ms // This delay time is necessary
    Set_LCD_RST;
    Delay_Ms(120);  // Delay 120 ms
    // Clr_LCD_CS;
    LCD_WR_REG(0x0011); // Exit Sleep
    LCD_WR_REG(0x00CF);  // Power Control B
    LCD_WR_DATA(0x0000); // Always 0x00
    LCD_WR_DATA(0x0081);  //
    LCD_WR_DATA(0X000c0);

    LCD_WR_REG(0x00ED); // Power on sequence control
    LCD_WR_DATA(0x0064); // Soft Start Keep 1 frame
    LCD_WR_DATA(0x0003); //
    LCD_WR_DATA(0X0012);
    LCD_WR_DATA(0X0081);

    LCD_WR_REG(0x00E8); // Driver timing control A
    LCD_WR_DATA(0x0085);
    LCD_WR_DATA(0x0001);
    LCD_WR_DATA(0x00798);
Initialization for the LT24 through IL9341 (2)

- LCD_WR_REG(0x00CB); // Power control A
  - LCD_WR_DATA(0x0039);
  - LCD_WR_DATA(0x002C);
  - LCD_WR_DATA(0x0000);
  - LCD_WR_DATA(0x0034);
  - LCD_WR_DATA(0x0002);

- LCD_WR_REG(0x00F7); // Pump ratio control
  - LCD_WR_DATA(0x0020);

- LCD_WR_REG(0x00EA); // Driver timing control B
  - LCD_WR_DATA(0x0000);
  - LCD_WR_DATA(0x0000);

- LCD_WR_REG(0x00B1); // Frame Control (In Normal Mode)
  - LCD_WR_DATA(0x0000);
  - LCD_WR_DATA(0x001b);

- LCD_WR_REG(0x00B6); // Display Function Control
  - LCD_WR_DATA(0x0000);
  - LCD_WR_DATA(0x0000);

- LCD_WR_REG(0x00C0); // Power control 1
  - LCD_WR_DATA(0x0005); //VRH[5:0]

- LCD_WR_REG(0x00C1); // Power control 2
  - LCD_WR_DATA(0x0011); //SAP[2:0];BT[3:0]

- LCD_WR_REG(0x00C5); //VCM control 1
  - LCD_WR_DATA(0x0045); //3F
  - LCD_WR_DATA(0x0045); //3C


Initialization for the LT24 through IL9341 (3)

- LCD_WR_REG(0x00C7); // VCM control 2
  - LCD_WR_DATA(0x00a2);

- LCD_WR_REG(0x0036); // Memory Access Control
  - LCD_WR_DATA(0x0008); // BGR order

- LCD_WR_REG(0x00F2); // Enable 3G
  - LCD_WR_DATA(0x0000); // 3Gamma Function Disable

- LCD_WR_REG(0x0026); // Gamma Set
  - LCD_WR_DATA(0x0001); // Gamma curve selected

- LCD_WR_REG(0x00E0); // Positive Gamma Correction, Set Gamma
  - LCD_WR_DATA(0x000F);
  - LCD_WR_DATA(0x0026);
  - LCD_WR_DATA(0x0024);
  - LCD_WR_DATA(0x00b);
  - LCD_WR_DATA(0x000E);
  - LCD_WR_DATA(0x0008);
  - LCD_WR_DATA(0x004b);
  - LCD_WR_DATA(0x00a8);
  - LCD_WR_DATA(0x003b);
  - LCD_WR_DATA(0x000a);
  - LCD_WR_DATA(0x0014);
  - LCD_WR_DATA(0x0006);
  - LCD_WR_DATA(0x0010);
  - LCD_WR_DATA(0x0009);
  - LCD_WR_DATA(0x0000);
Initialization for the LT24 through IL9341 (4)

- LCD_WR_REG(0x00E1);  //Negative Gamma Correction, Set Gamma
  - LCD_WR_DATA(0x0000);
  - LCD_WR_DATA(0x001c);
  - LCD_WR_DATA(0x0020);
  - LCD_WR_DATA(0x0004);
  - LCD_WR_DATA(0x0010);
  - LCD_WR_DATA(0x0008);
  - LCD_WR_DATA(0x0034);
  - LCD_WR_DATA(0x0047);
  - LCD_WR_DATA(0x0044);
  - LCD_WR_DATA(0x0005);
  - LCD_WR_DATA(0x000b);
  - LCD_WR_DATA(0x0009);
  - LCD_WR_DATA(0x002f);
  - LCD_WR_DATA(0x0036);
  - LCD_WR_DATA(0x000f);

- LCD_WR_REG(0x002A);  //Column Address Set
  - LCD_WR_DATA(0x0000);
  - LCD_WR_DATA(0x0000);
  - LCD_WR_DATA(0x0000);
  - LCD_WR_DATA(0x00ef);

- LCD_WR_REG(0x002B);  //Page Address Set
  - LCD_WR_DATA(0x0000);
  - LCD_WR_DATA(0x0000);
  - LCD_WR_DATA(0x0000);
  - LCD_WR_DATA(0x003f);

- LCD_WR_REG(0x003A);  //COLMOD: Pixel Format Set
  - LCD_WR_DATA(0x0055);
Initialization for the LT24 through IL9341 (5)

- LCD_WR_REG(0x00f6); // Interface Control
  LCD_WR_DATA(0x0001);
  LCD_WR_DATA(0x0030);
  LCD_WR_DATA(0x0000);

- LCD_WR_REG(0x0029); //display on

- LCD_WR_REG(0x002c); // 0x2C

- }
Camera interface
Ex: TRDB-D5M (Terasic)

From: TRDB-D5M_Hardware Specification
Camera basic Timing (TRDB-D5M)

- A 5Mpixels camera with 12 bits RGB
- 2592 x 1944 active rows from a
- 2752 x 2004 matrix
- Bayer colors Green1 – Red / Blue – Green2
Camera basic Timing (TRDB-D5M)
### Camera basic Timing (TRDB-D5M), Clock details

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Nominal voltages</th>
<th>11.5</th>
<th>17.7</th>
<th>19.1</th>
<th>ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>'CP</td>
<td>XCLKin to PIXCLK propagation delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>'PIXCLK</td>
<td>PIXCLK frequency</td>
<td></td>
<td>6</td>
<td>—</td>
<td>96</td>
<td>MHz</td>
</tr>
<tr>
<td>'PD</td>
<td>PIXCLK to data valid</td>
<td></td>
<td>0.6</td>
<td>1.2</td>
<td>2.2</td>
<td></td>
</tr>
<tr>
<td>'PFH</td>
<td>PIXCLK to FV HIGH</td>
<td></td>
<td>2.8</td>
<td>3.6</td>
<td>4.6</td>
<td></td>
</tr>
<tr>
<td>'PLH</td>
<td>PIXCLK to LV HIGH</td>
<td></td>
<td>2.2</td>
<td>3.2</td>
<td>4.2</td>
<td></td>
</tr>
<tr>
<td>'PFL</td>
<td>PIXCLK to FV LOW</td>
<td></td>
<td>2.4</td>
<td>3.4</td>
<td>4.2</td>
<td></td>
</tr>
<tr>
<td>'PLL</td>
<td>PIXCLK to LV LOW</td>
<td></td>
<td>2.6</td>
<td>3.4</td>
<td>4.2</td>
<td></td>
</tr>
<tr>
<td>CLOAD</td>
<td>Output load capacitance</td>
<td></td>
<td></td>
<td></td>
<td>&lt;10</td>
<td></td>
</tr>
<tr>
<td>CIN</td>
<td>Input pin capacitance</td>
<td></td>
<td></td>
<td>2.5</td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

---

![Timing Diagram](image)

*PLL disable for 'CP

FVAL leads LVAL by 609 PIXCLKs.

FVAL trails LVAL by 16 PIXCLKs.
## Camera basic Timing (TRDB-D5M)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Name</th>
<th>Equation</th>
<th>Default Timing at EXTCLK = 96 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>fps</td>
<td>Frame Rate</td>
<td>1/FRAME</td>
<td>15</td>
</tr>
<tr>
<td>HFRAME</td>
<td>Frame Time</td>
<td>(H + max(VB, VBMIN)) x tROW</td>
<td>66ms</td>
</tr>
<tr>
<td>HROW</td>
<td>Row Time</td>
<td>2 x tPIXCLK x max(((W/2) + max(HB, HBMIN)), (41 + 208 x (Row_Bin+1) + 99))</td>
<td>33.5μs</td>
</tr>
<tr>
<td>W</td>
<td>Output Image Width</td>
<td>2 x ceil((Column_Size + 1) / (2 x (Column_Skip + 1)))</td>
<td>2592 PIXCLK</td>
</tr>
<tr>
<td>H</td>
<td>Output Image Height</td>
<td>2 x ceil((Row_Size + 1) / (2 x (Row_Skip + 1)))</td>
<td>1944 rows</td>
</tr>
<tr>
<td>SW</td>
<td>Shutter Width</td>
<td>max(1, (2*16 * Shutter_Width_Upper + Shutter_Width_Lower))</td>
<td>1943 rows</td>
</tr>
<tr>
<td>HB</td>
<td>Horizontal Blanking</td>
<td>Horizontal_Blank + 1</td>
<td>1 PIXCLK</td>
</tr>
<tr>
<td>VB</td>
<td>Vertical Blanking</td>
<td>Vertical_Blank + 1</td>
<td>26 rows</td>
</tr>
<tr>
<td>HBMIN</td>
<td>Minimum Horizontal Blanking</td>
<td>208 x (Row_Bin + 1) + 64 + (WDC/2)</td>
<td>312 PIXCLK</td>
</tr>
<tr>
<td>VBMIN</td>
<td>Minimum Vertical Blanking</td>
<td>max(8, SW - H) + 1</td>
<td>9 rows</td>
</tr>
<tr>
<td>tPIXCLK</td>
<td>Pixclk Period</td>
<td>1/tPIXCLK</td>
<td>10.42ns</td>
</tr>
</tbody>
</table>
## Camera Standard Resolution (TRDB-D5M)

<table>
<thead>
<tr>
<th>Resolution</th>
<th>Frame Rate</th>
<th>Sub-sampling Mode</th>
<th>Column Size (R0x04)</th>
<th>Row Size (R0x03)</th>
<th>Shutter-Width-Lower (R0x09)</th>
<th>Row_Bin (R0x22 [5:4])</th>
<th>Row_Skip (R0x22 [2:0])</th>
<th>Column_Bin (R0x23 [5:4])</th>
<th>Column_Skip (R0x23 [2:0])</th>
</tr>
</thead>
<tbody>
<tr>
<td>2592 x 1944 (Full Resolution)</td>
<td>15.15</td>
<td>N/A</td>
<td>2591</td>
<td>1943</td>
<td>&lt;1943</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2,048 x 1,536 QXGA</td>
<td>23</td>
<td>N/A</td>
<td>2047</td>
<td>1535</td>
<td>&lt;1535</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1,600 x 1,200 UXGA</td>
<td>35.2</td>
<td>N/A</td>
<td>1599</td>
<td>1199</td>
<td>&lt;1199</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1,280 x 1,024 SXGA</td>
<td>48</td>
<td>N/A</td>
<td>1279</td>
<td>1023</td>
<td>&lt;1023</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>48</td>
<td>skipping</td>
<td>2559</td>
<td>2047</td>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>40.1</td>
<td>binning</td>
<td>2559</td>
<td>2047</td>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1,024 x 768 XGA</td>
<td>73.4</td>
<td>N/A</td>
<td>1023</td>
<td>767</td>
<td>&lt;767</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>73.4</td>
<td>skipping</td>
<td>2047</td>
<td>1535</td>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>59.7</td>
<td>binning</td>
<td>2047</td>
<td>1535</td>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>800 x 600 SVGA</td>
<td>107.7</td>
<td>N/A</td>
<td>799</td>
<td>599</td>
<td>&lt;599</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>107.7</td>
<td>skipping</td>
<td>1599</td>
<td>1199</td>
<td></td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>85.2</td>
<td>binning</td>
<td>1599</td>
<td>1199</td>
<td></td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>640 x 480 VGA</td>
<td>150</td>
<td>N/A</td>
<td>639</td>
<td>479</td>
<td>&lt;479</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>150</td>
<td>skipping</td>
<td>2559</td>
<td>1919</td>
<td></td>
<td>0</td>
<td>3</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>77.4</td>
<td>binning</td>
<td>2559</td>
<td>1919</td>
<td></td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>3</td>
</tr>
</tbody>
</table>
FPGA architecture

- NIOSII
- EPCS Ctrl
- JTAG UART
- Camera Ctrl
- SDRAM Ctrl
- SRAM
- ... (ellipsis)
- i2c

Avalon bus
Camera Controller architecture

Avalon Master

- Burst transfers

Avalon Slave

- Start Address
- Length
- Start

Camera Interface

- FIFO
- Mode
- Start
- Stop

- Start Address
- Length
- Start

Avalon

- 32 bits
- 4 pixels/transfer

- NewData
- DataAck
- NewFrame

Data

- HSync
- VSync
- MClk

RB 2006/A2015
As a master, burst access allows the transfer of uninterruptable data flow.

The **BurstCount** is provided by the master unit and the number of announced data has to be provided.
Camera Interface, signals

- Camera interface:
  - Mclk: Cam_Mclk
  - HSync: Cam_HSync
  - VSync: Cam_VSync
  - CamData[7..0]: Cam_data[7..0]
  - CamReset_n: Cam_Reset_n

- Slave interface → interface programmation:
  - Clk: Clk
  - Address: AS_Address[2..0]
  - CSelect: AS_Cs_n
  - Write: AS_Write_n
  - DataWrite[31..0]: AS_Datawr[31..0]
  - Read: AS_Read_n
  - DataRead[31..0]: AS_Datard[31..0]
  - InterruptRequest: AS_IRQ_n

- Master interface → Data transfers to memory:
  - Clk: Clk
  - Address [31..0]: AM_Address[31..0]
  - ByteEnable_n[3..0]: AM_ByteEnable_n[3..0]
  - BurstCount: AM_BurstCount[2..0]
  - Write: AM_Write_n
  - DataWrite[31..0]: AM_Datawr[31..0]
  - WaitRequest: AM_WaitRequest
### Camera Interface, slave access: internal registers

<table>
<thead>
<tr>
<th>Address</th>
<th>Register</th>
<th>Rz value</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>00h</td>
<td>CamAddr</td>
<td>0h</td>
<td>32</td>
<td>Destination Address</td>
</tr>
<tr>
<td>04h</td>
<td>CamLength</td>
<td>128*101</td>
<td>24</td>
<td>Buffer size in bytes</td>
</tr>
<tr>
<td>08h</td>
<td>CamComm</td>
<td>00h</td>
<td>8</td>
<td>Command</td>
</tr>
<tr>
<td>0Ch</td>
<td>CamStatus</td>
<td>00h</td>
<td>8</td>
<td>Status</td>
</tr>
<tr>
<td>10h</td>
<td>CamStart</td>
<td>0</td>
<td>8</td>
<td>Acquisition enabled</td>
</tr>
<tr>
<td>14h</td>
<td>CamStop</td>
<td>0</td>
<td>8</td>
<td>Stop acquisition</td>
</tr>
<tr>
<td>18h</td>
<td>CamSnapshot</td>
<td>0</td>
<td>8</td>
<td>Snapshot, activate VSync</td>
</tr>
</tbody>
</table>
Camera Registers (TRDB-D5M)

- 256 internal registers available through i2c
- ~40 used
- Clock programming
- Frame programming
I^2c (TRDB-D5M)

- I^2c transfers
- Addresses:
  - 0xBA: write ‘1011 1010’
  - 0xBB: read ‘1011 1011’
- 400 kHz
- Register Address on 8 bits
Camera to work (TRDB-D5M), External Clk mode

- Activate Reset_n
- Power On
- Desactivate Reset_n
- External Clock provided
  - XClkIn: 6 .. 96 MHz Clock to be provided
  - $f_{PixClk} = f_{XClkIn}$ if Divide_Pixel_Clock = 0
  - $f_{PixClk} = f_{XClkIn}/(2 \times \text{Divide\_Pixel\_Clock})$
Camera to work (TRDB-D5M), PLL mode

- PLL pixel clk generation
- fXClkln: 6MHz .. 27MHz
- Power PLL
- Set M, N, P1

\[ \text{f}_{\text{PIXCLK}} = \left( \text{f}_{\text{XCLKIN}} \times M \right) / \left( N \times P1 \right) \]

The PLL control registers must be programmed while the sensor is in the software Standby state. The effect of programming the PLL divisors while the sensor is in the streaming state is UNDEFINED.
Camera to work (TRDB-D5M), PLL mode

- PLL pixel clk generation
- $f_{XClkIn}: 6\text{MHz} .. 27\text{MHz}$
- Power PLL
- Set M, N, P1
  \[ f_{\text{PIXCLK}} = \left( \frac{f_{\text{XCLKIN} \times M}}{N \times P1} \right) \]
- $2\text{MHz} < \frac{f_{XClkIn}}{N} < 13.5\text{MHz}$
- $180\text{MHz} < \left( \frac{f_{XClkIn} \times M}{N} \right) < 360\text{MHz}$
- M: 16..255
- Use_PLL \((\text{Reg0x10[1] = 1})\) from XClkIn to PLL mode
Camera to work (TRDB-D5M), Skipping

- Skipping of line/column

Figure 3.3: Pixel Readout (no skipping)

Figure 3.4: Pixel Readout (Column Skip 2X)

Figure 3.5: Pixel Readout (Row Skip 2X)

Figure 3.6: Pixel Readout (Column Skip 2X, Row Skip 2X)
Camera to work (TRDB-D5M), Binning

- Binning of line/column

Figure 3.7: Pixel Readout (Column Bin 2X)  Figure 3.8: Pixel Readout (Column Bin 2X, Row Bin 2X)
Camera Interface, signals

- **Camera interface:**
  - Camera interface: Dir, FPGA view
    - Pixel_Clk (PixClk) In (from Camera to FPGA)
    - LineValid (Cam_Lval) In
    - FrameValid (Cam_Fval) In
    - CamData[11..0] (Cam_data[11..0]) In
    - CamReset_n (Cam_Reset_n) Out
    - Strobe In
    - Trigger In
    - XCLKIN Out

- **Slave interface → interface programmation**
  - Clk In
  - Address AS_Address[2..0] In
  - CSelect AS_Cs_n In
  - Write AS_Write_n In
  - DataWrite[31..0] AS_DataWr[31..0] In
  - Read AS_Read_n In
  - DataRead[31..0] AS_DataRd[31..0] Out
  - InterruptRequest AS_IRQ_n Out

- **Master interface → Data transfers to memory:**
  - Clk In
  - Address [31..0] AM_Address[31..0] Out
  - ByteEnable_n[3..0] AM_ByteEnable_n[3..0] Out
  - BurstCount AM_BurstCount[2..0] Out
  - Write AM_Write_n Out
  - DataWrite[31..0] AM_DataWr[31..0] Out
  - WaitRequest AM_WaitRequest In
Camera Interface, signals on Avalon Master

- As a master, burst access allows the transfer of uninterruptable data flow
- The **BurstCount** is provided by the master unit and the number of announced data has to be provided.
Another LCD: TX-07
Another Protocol
This kind of LCD is controlled by a parallel data flow: **RGB** digital intensity.

It's synchronized at Frame level with **Vertical Synchronization : VSync**

It's synchronized at Line level with **Horizontal Synchronization : HSync**

It's synchronized by a Clock at pixel level: **DotClk**
TX07 TFT_LCD

Diagram of TX07 TFT_LCD circuit with connections and components.
Interface with TFT-LCD

- Some Voltage need to be generated for the LCD:
  - VGH/VGL @+/- 15V for internals +13V/-5V
  - Vcc @ 3V
  - VDH @ 5V
  - VCOM @ ~2.2V
- A DotClk @ 5 ~12 MHz
TX07 Synchronization
TX07 Synchronization

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>MIN.</th>
<th>TYP.</th>
<th>MAX.</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Back porch for Horizontal</td>
<td>HBP</td>
<td>-</td>
<td>12</td>
<td>Clock</td>
</tr>
<tr>
<td>Front porch for Horizontal</td>
<td>HFP</td>
<td>15</td>
<td>18 Note(1)</td>
<td>21</td>
</tr>
<tr>
<td>Back porch for Vertical</td>
<td>VBP</td>
<td>-</td>
<td>8 Note(3)</td>
<td>-</td>
</tr>
<tr>
<td>Front porch for Vertical</td>
<td>VFP</td>
<td>17</td>
<td>(20) Note(2)</td>
<td>22</td>
</tr>
</tbody>
</table>

Note(1) : (DOTCLK total) - ((Valid data period for Horizontal) + (HBP))
(2) : (HSYNC total) - ((Active Area period) + VBP)
Extension for FPGA4U

• An extension board for FPGA4U allows connection of 2 different LCD from Hitachi:
  - TX06
    - http://www.hitachi-displays-eu.com/doc/TX06D57VM0AAA.pdf
  - TX07

• And a VGA interface with a DAC
ExtLCD for FPGA4U

SD/MMC subsystem

LCD subsystem

VGA subsystem

64 pin connector from FPGA4U

SD/MMC Flash card

Data bus

DAC

VGA

To monitor
Avalon Slave, registers

- **FBufAdd**, Address of the frame buffer to display
- **FBLgt**, Length of the frame buffer (in pixels number, 240 x 320 by default)
- **DisplayCom**, Command (Enable display, IRQ at end of Frame, Power Control)
- **DisplayStat**, Status (Run, EOF (End Of frame))
- **HBP** (Horizontal Back Porch) (default: 12)
- **HFP** (Horizontal Front Porch): (default: 18)
- **VBP** (Vertical Back Porch): (default: 8)
- **VFP** (Vertical Front Porch) : (default: 20)
- **HData** (Horizontal Data) : (default: 240)
- **VData** (Vertical Data) : (default: 320)
- ...
### Avalon Slave, registers mapping

<table>
<thead>
<tr>
<th>Add. (Offset)</th>
<th>Name</th>
<th>Reset Val.</th>
<th>Function</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>FBAdd</td>
<td>0</td>
<td>Address of the frame buffer to display</td>
<td>32</td>
</tr>
<tr>
<td>0x1</td>
<td>FBLgt</td>
<td>240 x 320</td>
<td>Length of the frame buffer in pixels</td>
<td>32</td>
</tr>
<tr>
<td>0x2</td>
<td>DisplayCom</td>
<td>0</td>
<td>Command (Start, Stop, IRQ, Power )</td>
<td>8</td>
</tr>
<tr>
<td>0x3</td>
<td>DisplayStat</td>
<td>0</td>
<td>Status (Run, EOF (End Of frame))</td>
<td>8</td>
</tr>
<tr>
<td>0x4</td>
<td>HBP</td>
<td>12</td>
<td><em>Horizontal Back Porch</em> (Nb DotClk)</td>
<td>16</td>
</tr>
<tr>
<td>0x5</td>
<td>HFP</td>
<td>18</td>
<td><em>Horizontal Front Porch</em> (Nb DotClk)</td>
<td>16</td>
</tr>
<tr>
<td>0x6</td>
<td>VBP</td>
<td>8</td>
<td><em>Vertical Back Porch</em> (Nb Lines)</td>
<td>16</td>
</tr>
<tr>
<td>0x7</td>
<td>VFP</td>
<td>20</td>
<td><em>Vertical Front Porch</em> (Nb Lines)</td>
<td>16</td>
</tr>
<tr>
<td>0x8</td>
<td>HData</td>
<td>240</td>
<td><em>Horizontal Data</em> (Nb DotClk)</td>
<td>16</td>
</tr>
<tr>
<td>0x9</td>
<td>VData</td>
<td>320</td>
<td><em>Vertical Data</em> (Nb Lines)</td>
<td>16</td>
</tr>
<tr>
<td>0xA</td>
<td>HSync</td>
<td>2</td>
<td>Horizontal Sync Length (Nb DotClk)</td>
<td>16</td>
</tr>
<tr>
<td>0xB</td>
<td>VSync</td>
<td>7</td>
<td>Vertical Sync Length (Nb Lines)</td>
<td>16</td>
</tr>
<tr>
<td>0xC</td>
<td></td>
<td></td>
<td></td>
<td>68</td>
</tr>
</tbody>
</table>
Power control

- 3 signals allows control of Power on the LCD module. They have to be controlled by the module as 3 Ports bits.
- The DisplayCom register controls them
- **StepUp_ON**:  
  - Allows internal +5V generation, necessary for VGA and LCD on 45 pins connector
- **LED_ON**:  
  - Allows LED back light ON
- **LCD_ON**:  
  - Needed for LCD TX07 to work
The LCD Control part sends the synchronization signals to the LCD:

- VSync
- HSync
- DotClk
- RGB (3x6 bits/pixel)

- Read the pixels data from FIFO
- Receive information from Avalon slave part through registers interface
- It contains counters for signals and timing generation
- It's based on a state machine to control them
LCD Controller : FIFO

- Writing of data from the Master interface and reading from LCD control have to be perfectly synchronized.
- Read access from SDRAM memory can **not** be guaranties at pixel level timing.
- We have to guaranty that the global data flow is possible and with which delay!
- A FIFO is an excellent way to allow synchronization between 2 asynchronous units.
LCD Controller : FIFO

• Rules:
  ➢ The Avalon master try to fulfill the FIFO when it can
  ➢ The LCD control unit read it when it needs.

• To be efficient, the Avalon master try to make consecutive reads, thus the SDRAM controller can do burst transfers.

• The FIFO needs to provide an information to the Avalon master module when it has a minimum of empty positions as a multiple of the burst transfers (4, 8, 16, .. ).

• The FIFO send information to the LCD Control module when it has at least 1 available pixel data.
Global questions

- Format of the bitmap in memory
- Color organization
- Pixel resolution
Memory ↔ Display relation

FBAdd

FBLgt

Line 0

Line 1

Line 319

240 columns each

Line 0

240 columns each

Line 319

240 columns each
Pixel organization, some choices

• 1 pixel organization:
  ➢ 18 bits/pixel at LCD
  ➢ Ex. 32 bits /pixel at memory
  ➢ RGB or BGR ?
  ➢ 6 bits / Byte: right or left alignment ?
Pixel organization, some choices

• 1 pixel organization:
  ➢ 18 bits/pixel at LCD
  ➢ Ex. **16** bits/pixel at memory, 2 pixels / 32 bits
  ➢ RGB or BGR ?
  ➢ **5-6-5** bits / doublet: RGB, 2 bits lost
  ➢ **5-5-5** bits / doublet: RGB, 3 bits lost
Pixel organization

• Many choices

• Need to be done!

• More bits/pixel 18 on 32 bits →
  ➢ more memory for a frame
  ➢ more bandwidth necessary
  ➢ more colors available $2^{18} : 262144$
  ➢ Memory space free for other function

• Less bits/pixel (16)
  ➢ Lost in color resolution 15 bits → 32’768
  ➢ 16 bits 65’536, more on Green generally